USB PD Sink Controller Supporting EPR Mode

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HUSB238A

FEATURES

- Fully Autonomous USB Type-C® and USB PD Sink Controller
- Compliant USB Type-C® Specification Reversion 2.1 and USB PD Specification Reversion 3.1
- Hardware Configurable for FPDO Request
- APDO, EPR PDO Supported through I²C Configuration
- Automatic Legacy Protocols Detection including BC1.2, Divider 3, QC2.0
- Support SOP' Detection
- Typical Low Power Operation: I_{VDD}< 45 μA
- Integrated VBUS Switch Driver
- Dead Battery Support
- VBUS over-voltage protection (OVP) and under-voltage protection (UVP)
- Over-temperature protection (OTP) with programmable thresholds
- 4 kV HBM ESD Rating for USB IO pins
- Small Package, 16 Lead QFN (3 mm x 3 mm)

APPLICATIONS

PD sink devices

USB-C cables

Wireless charger

GENERAL DESCRIPTION

The HUSB238A is a highly integrated stand-alone USB Type-C® and Power Delivery (PD) Sink controller. The HUSB238A integrates the CC logic, USB PD protocol and the legacy protocols.

The HUSB238A can run in I²C mode and GPIO mode. In I²C mode, an I²C master can access the HUSB238A to configure settings, read back status and perform advanced functions such as DR Swap, VDM messages. While in GPIO mode, the configuration is achieved via the setting pins.

The ultra-low operation current of the HUSB238A helps the system to reduce the total power dissipation and suitable for a battery application.

The HUSB238A is available in QFN 3 mm x 3 mm-16L package.

TYPICAL APPLICATION CIRCUIT

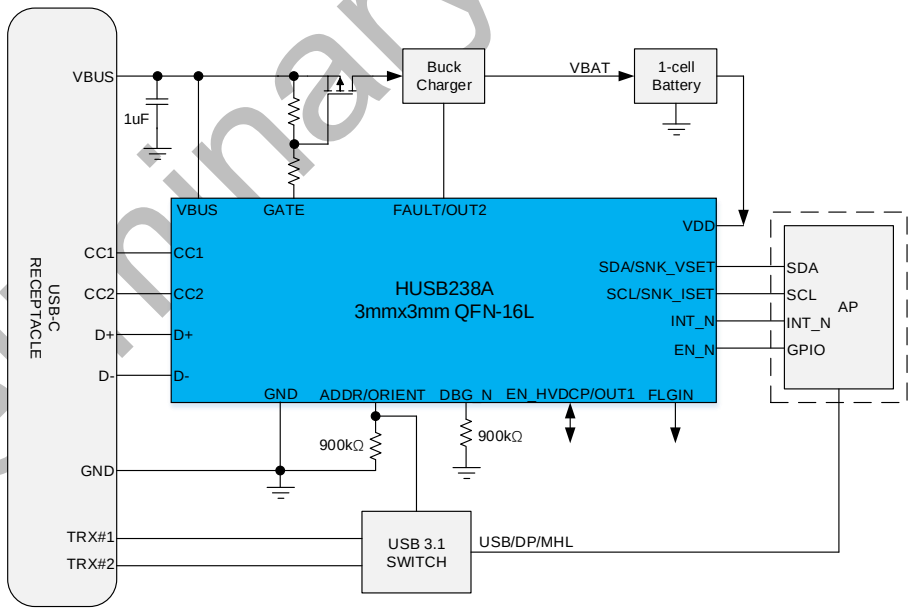

Figure 1. Typical Application Circuit

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REVISION HISTORY

Version	Date	Descriptions
Rev. 0.1	05/2023	Initial version

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

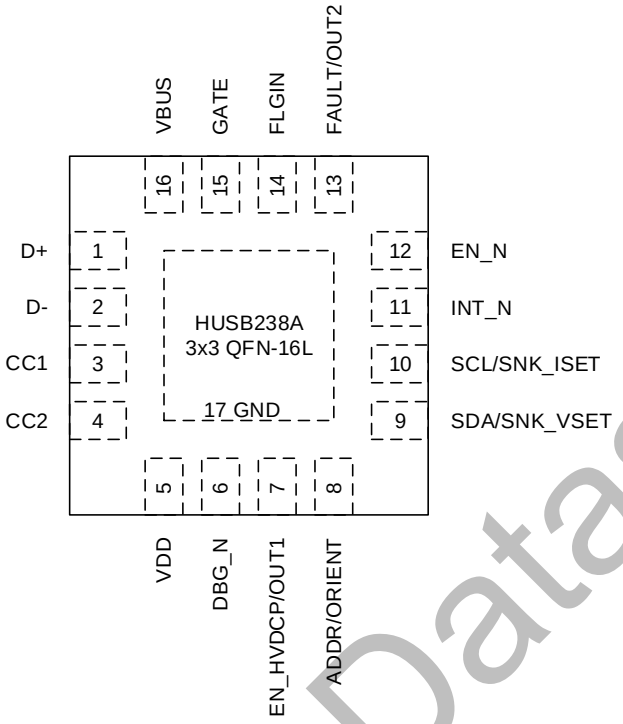


Figure 2. Pin Assignment

Table 1. Pin Function Descriptions

Pin No.	Pin Name	Type1	Description
1	D+	IO	Positive line of the USB data line pair.
2	D−	IO	Negative line of the USB data line pair.
3	CC1	IO	USB Type-C CC1 line.
4	CC2	IO	USB Type-C CC2 line.
5	VDD	P	Input supply 1 for internal circuitry. It is recommended to tie this pin to the single cell battery or a 3.3 V power rail. When the power is not available this pin, the VBUS pin may power the internal circuitry. Place a 1μF ceramic capacitor across this pin and GND pin.
6	DEBUG_N	IO	This pin is push-pull output to indicate the Debug Accessory Detection results. Low = Debug Accessory detected High = Debug Accessory not detected Note: a 900 kΩ resistor to GND should be used.
7	EN_HVDCP/OUT1	IO	Dual function pin. In input mode, this pin (EN_HVDCP) is a digital input pin to enable the HVDCP protocol detection in Sink mode. HUSB238A may perform different actions: Connected to GND = Only perform BC1.2 detection Connected to VDD = Perform HVDCP detection after BC1.2 DCP is detected In output mode, this pin (OUT1) is push-pull output whose output status can be configured by I^2C. Note: a 900 kΩ resistor should be used when connecting to VDD or GND to reduce standby current.
8	ADDR/ORIENT	IO	Dual function pin. In input mode, this pin (ADDR) is a 3 state input to set the working mode. The working mode is defined as:

Pin No.	Pin Name	Type1	Description
			Connected to VDD = I²C mode with slave address 62H Connected to GND = I²C mode with slave address 42H Float = GPIO mode In output mode, this pin (ORIENT) is push-pull output to indicate the connection status. Low = CC1 of USB Type-C receptacle is connected High = CC2 of USB Type-C receptacle is connected Note: a 900 kΩ resistor should be used when connecting to VDD or GND to reduce standby current.
9	SDA/SNK_VSET	AIO	Dual functions pin. In I²C mode, this pin (SDA) is the data line of I²C bus. In GPIO mode, this pin (SNK_VSET) combined with SNK_ISET to determine the requested voltage.
10	SCL/SNK_ISET	AIO	Dual functions pin. In I²C mode, this pin (SDA) is the clock line of I²C bus. In GPIO mode, this pin (SNK_ISET) combined with SNK_VSET to determine the requested current.
11	INT_N	AIO	In I²C mode, this pin (INT_N) is an open-drain output to request the attention of processor by pulling down this pin.
12	EN_N	AI	Chip enabled pin. It is pulled up internally and HUSB238A is enabled by pulling this pin to GND.
13	FAULT/OUT2	DO	General output pin. The output purpose can be configured as a FAULT pin. When used as FAULT pin, the device pulls this pin high if the power adapter cannot supply the required voltage or current or if an OVP/UVP/OTP event is detected. This pin can be also configured as General output pin (OUT2) controller by I²C master.
14	FLGIN	DI	General input pin. This input signal can be used to disable the GATE driver and generate an interrupt when there is a valid high voltage is detected. It can be also configured as just an interrupt source for INT_N, not disabling GATE driver.
15	GATE	O	Open drain output. This pin is employed to control the external VBUS switch.
16	VBUS	P	This pin has multiple functions including VBUS voltage detection, the discharge path for VBUS pin and the Input supply 2 for internal circuitry. When VDD is unpowered, HUSB238A could consume power from this pin.
17	GND	P	Ground connection point

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

RECOMMENDED OPERATING CONDITIONS

Table 2.

Parameter	Rating
VDD Input Voltage	3 V to 5.5 V
VBUS Input Voltage (VDD is available)	3.15 V to 29.4 V
VBUS Input Voltage (VDD is unavailable)	4.5 V to 29.4 V
Operating Temperature Range (Junction)	-40 °C to 125 °C
Ambient Temperature Range	-40 °C to 85 °C

SPECIFICATIONS

V_{DD} = 3 V to 5.5 V or V_{DD} < 3 V and VBUS = 4.5 V to 29.4 V, T_J = -40 °C to 125 °C for minimum and maximum specifications, and T_A = 25 °C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply						
VDD UVLO Rising Threshold	$V_{DD\_UVLO\_R}$	Power Up to normal operation	2.65	2.75	2.85	V
VDD UVLO Falling Threshold	$V_{DD\_UVLO\_F}$	Falling edge to stop normal operation	2.55	2.65	2.75	V
VDD UVLO Hysteresis	$V_{DD\_UVLO\_HYS}$	Hysteresis Voltage to be shutdown		0.1		V
VDD Standby Current	I_{STBY}	EN_N=Low without attachment, VDD=4.5 V & VBUS=0 V		30	45	μA
VDD Operating Current in Active Mode	I_{OP_VDD}	EN_N=Low and attached as an Active Sink, VDD=4.5 V & VBUS=5 V		4	4.5	mA
VBUS UVLO Threshold	$V_{BUS\_UVLO\_R}$	VDD=0 V	3.67	4	4.4	V
	$V_{BUS\_UVLO\_F}$	VDD=0 V	2.9	3.3	3.67	V
VBUS UVLO Hysteresis	$V_{BUS\_UVLO\_HYS}$	Hysteresis Voltage to be shutdown		0.1		V
VBUS Operating Current in Active Mode	I_{OP_VBUS}	EN_N=Low and attached as an Active Sink, VDD=0 V & VBUS=29.4 V		4	4.5	mA
Open Drain Output Pins (GATE, INT_N)						
Output Low Voltage	V_{OL_OD}	Sink current=2 mA			0.4	V
Enable Pin (EN_N)						
Low Level Input Threshold	V_{IL_EN}				0.4	V
High Level Input Threshold	V_{IH_EN}		1.35			V
Input and Output Pins (PORT/DEBUG_N, ADDR/ORIENT, EN_HVDCP/OUT1)						
Output Low Voltage	V_{OL_PP}	Sink current=1 mA			$0.2 \cdot V_{DD}$	V
Output High Voltage	V_{OH_PP}	Source current=1 mA	$0.8 \cdot V_{DD}$			V
I^2C Characteristics (SDA, SCL pins)						
Output Low Voltage	V_{OL_I2C}	Sink current is 2 mA			0.4	V
Input Low Voltage	V_{IL_I2C}	I^2C Pull up voltage is 3.3 V			0.99	V
Input High Voltage	V_{IH_I2C}	I^2C Pull up voltage is 3.3 V	2.31			V
Input Voltage Hysteresis	V_{HYS_I2C}	I^2C Pull up voltage is 3.3 V	0.17			V
SCL Clock Frequency	f_{SCL_I2C}		0		400	kHz
Analog Input Pins (SNK_ISET, SNK_VSET, SRC_ISET)						

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Pull up Source Current	I_{SNK_VSET}	On SNK_VSET pin	95	100	105	μA
	I_{SNK_ISET}	On SNK_ISET pin	95	100	105	μA
SNK_VSET Setting Resistor	R_{SNK_VSET0}		0		2	kΩ
	R_{SNK_VSET1}		2.85	3	3.15	kΩ
	R_{SNK_VSET2}		5.7	6	6.3	kΩ
	R_{SNK_VSET3}		10.45	11	11.55	kΩ
	R_{SNK_VSET4}		18.05	19	19.95	kΩ
	R_{SNK_VSET5}		1			MΩ
SNK_VSET Setting Resistor	R_{SNK_ISET0}		0		1.5	kΩ
	R_{SNK_ISET1}		2.137	2.25	2.362	kΩ
	R_{SNK_ISET2}		3.8	4	4.2	kΩ
	R_{SNK_ISET3}		5.7	6	6.3	kΩ
	R_{SNK_ISET4}		7.98	8.4	8.82	kΩ
	R_{SNK_ISET5}		10.925	11.5	12.075	kΩ
	R_{SNK_ISET6}		14.82	15.6	16.38	kΩ
	R_{SNK_ISET7}		19.95	21	22.05	kΩ
	R_{SNK_ISET8}		1			MΩ
Type-C Pins (CC1, CC2)						
Sink Pull Down Resistor	R_d	In Sink Mode	4.6	5.1	5.6	kΩ
R_a Detection Threshold as Sink	vR_{a_SNK}	Connected as Sink	0.15	0.2	0.25	V
R_d Detection Threshold as Sink	vR_{d_SNKDEF}	Connected as Sink with I_{RP_DEF} attached	0.61	0.66	0.7	V
	$vR_{d\_SNK1.5A}$	Connected as Sink with $I_{RP\_1.5A}$ attached	1.16	1.23	1.31	V
CC Over-voltage Threshold	v_{CCOV}	For any CC pin, VDD > $V_{DD\_UVLO\_R}$		V_{DD}+3		V
		For any CC pin, VDD < $V_{DD\_UVLO\_F}$		6.3		V
VBUS Present and Protection						
VBUS Present Rising Threshold	vVB_{PRS_R}	Rising edge to set VBUS_OK=1b	3.67	4	4.4	V
VBUS Present falling Threshold	vVB_{PRS_F}	Falling edge to set VBUS_OK=0b	2.9	3.3	3.67	V
VBUS Present Hysteresis	vVB_{PRS_HYS}	Hysteresis Voltage to set VBUS_OK=0b		0.7		V
VBUS UV falling Threshold	vVB_{UV_F0}	Falling edge to detect disconnection when 26 V > RDO > 10 V, refer to the requested voltage		86		%
	vVB_{UV_F1}	Falling edge to detect disconnection when 10 V ≥ RDO > 5 V, refer to the requested voltage		80		%
	vVB_{UV_F2}	Falling edge to detect disconnection when RDO ≥ 26 V		22.4		V
VBUS UV Hysteresis	vVB_{UV_HYS}			0.1		V
VBUS Over-voltage Threshold	V_{BUS_OV}	Refer to the requested voltage		120		%
VBUS Over-voltage Hysteresis	vVB_{OV_HYS}			0.1		V
VBUS Over-voltage Deglitch	t_{DEB_OV}	Valid duration to set interrupt		50		μs
BC1.2 and HVDCP Detection						
DCD source current	I_{DP_SRC}		7	10	13	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DCD Timeout	$t_{DCD\_TIMEOUT}$			500		ms
BC1.2 Source voltage	$V_{DPM\_SRC\_0V6}$		0.5	0.6	0.7	V
BC1.2 Sink Current	I_{DPM_SNK}		50	100	150	μA
D- Source Voltage for 3.3V	$V_{DM\_SRC\_3P3}$		3.0	3.3	3.6	V
D+ Source Voltage for 3.3V	$V_{DP\_SRC\_3P3}$		3.0	3.3	3.6	V
D- 3.3V Pull-up Resistance	$R_{DM\_SRC\_3P3}$		0.9	1.24	1.57	kΩ
D+ 3.3V Pull-up Resistance	$R_{DP\_SRC\_3P3}$		0.9	1.24	1.57	kΩ
Data Detect Voltage	V_{DAT_REF}		250	325	400	mV
D+/D- Comparator Threshold for 2.7V Detection	$V_{TH\_2P7\_HI}$	High threshold for Apple divider 3	2.85	2.95	3.05	V
	$V_{TH\_2P7\_LO}$	Low threshold for Apple divider 3	2.25	2.35	2.45	V
Digital Input Pin (FLGIN)						
Digital Input High Voltage	V_{IH_GPIO}	VI_GPIO for 3.3 V	2			V
Digital Input Low Voltage	V_{IL_GPIO}	VI_GPIO for 3.3 V			0.8	V
Input Hysteresis	V_{HYS_GPIO}	VI_GPIO for 3.3 V	0.2			V
Digital Output Pin (FAULT/OUT2)						
Output Low Voltage	V_{OL_PP}	Sink current=1 mA			$0.2V_{DD}$	V
Output High Voltage	V_{OH_PP}	Source current=1 mA	$0.8V_{DD}$			V
Thermal Shut Down						
Thermal Shut Down Threshold	T_{TSD_R}	Rising Threshold		150		℃
	T_{TSD_F}	Falling Threshold		130		℃
TSW Debounce Time	t_{DB_TSW}			100		ms
TSD Debounce Time	t_{DB_TSD}			1000		ms

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VBUS, GATE, CC1, CC2	−0.3 V to 33 V
D+, D−, ADDR/ORIENT, VDD, INT_N, SDA/SNK_VSET, SCL/SNK_ISET, EN_HVDCP/OUT1, FLGIN, EN_N, FAULT/OUT2, DBG_N	−0.3 V to 7 V
Operating Temperature Range (Junction)	−40 °C to 125 °C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model (VBUS, CC1, CC2, D+ and D- pins)	±4000 V
Human Body Model (other pins)	±2000 V
Charged Device Model	±500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN3x3-16L	70	41	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

FUNCTIONAL BLOCK DIAGRAM

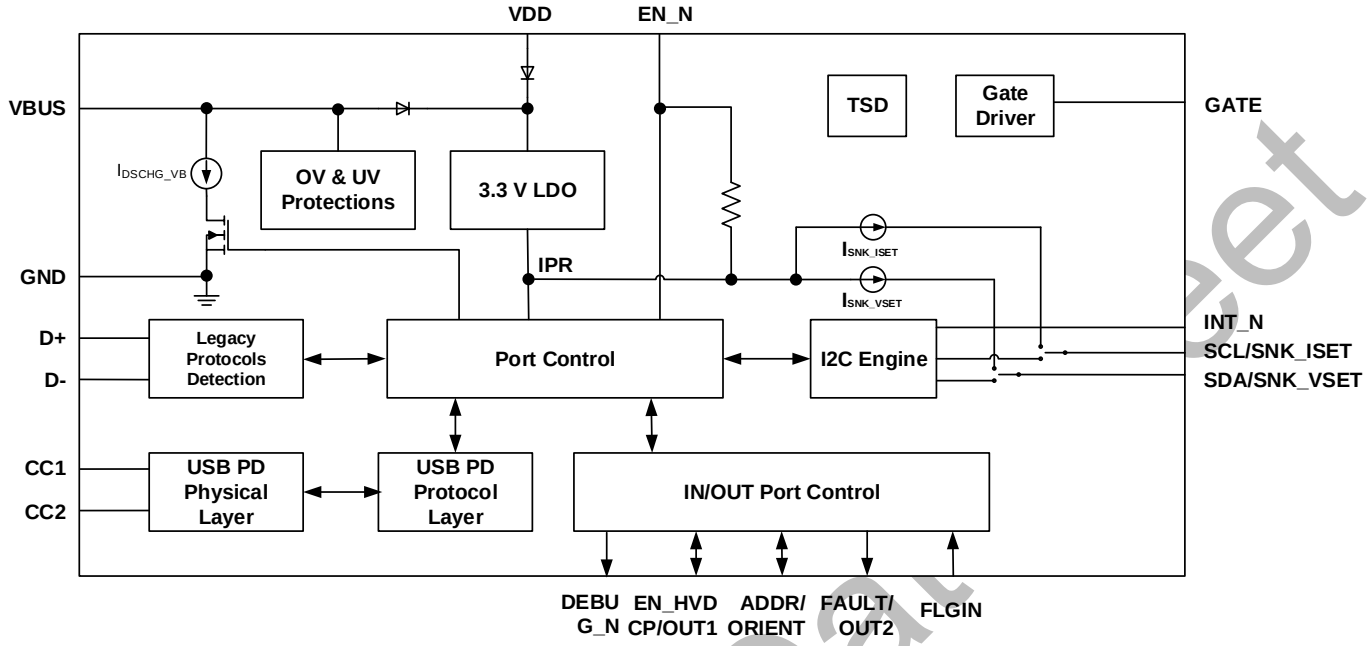


Figure 3. Functional Block Diagram

THEORY OF OPERATION

The HUSB238A is a USB PD Sink controller. It supports PD protocol and legacy charging protocols detection and requests the desired power per the user settings. The HUSB238A can run in I2C mode and GPIO mode. In I2C mode, an I2C master can access the HUSB238A to configure settings, read back status and perform advanced functions such as DR Swap, VDM messages. While in GPIO mode, the configuration is achieved via the setting pins.

POR AND UVLO

HUSB238A can be powered by VDD pin or VBUS pin. The VDD pin has higher priority. When the voltage at VDD pin exceeds the $V_{DD\_UVLO\_R}$ or the VBUS voltage exceeds the $V_{BUS\_UVLO\_R}$ when VDD < $V_{DD\_UVLO\_F}$, HUSB238A starts initialization.

When the voltage at VDD pin is less than $V_{DD\_UVLO\_F}$ and VBUS voltage is less than $V_{BUS\_UVLO\_F}$, the HUSB238A is reset.

ENABLE CONTROL

HUSB238A has an enable pin (EN_N) for the whole system control. When EN_N is high, the whole system is disabled, When EN_N is low, the whole system is enabled.

When EN_N is low, and HUSB238A is in I²C mode, there is an additional ENABLE bit (Register CONTROL1[3]) to enable or disable the HUSB238A, when this ENABLE bit is 0b, all of functions of HUSB238A is turned off except the I²C accessibility, EN_N detection and UVLO detection. Only when the ENABLE=1b, the disabled functions resume to work.

ADDR/ORIENT PIN

For ADDR/ORIENT pin, it is employed to select whether HUSB238A works as I²C mode or GPIO mode.

Table 6. Work Mode Configuration

ADDR/ORIENT Connection	HUSB238A Work Mode Configured
Connected to VDD via a 900kΩ Resistor	I²C mode with slave address=62H
Floating	GPIO mode
Connected to GND via a 900kΩ Resistor	I²C mode with slave address=42H

EN_HVDCP/OUT1 PIN

For EN_HVDCP/OUT1 pin, it is employed to determine whether HUSB238A can support HVDCP detection.

Table 7. Legacy Protocol Detection Configuration

EN_HVDCP/OUT1 Connection	HUSB238A Legacy Protocol Detection
Connected to VDD via a 900kΩ Resistor	Perform BC1.2 and HVDCP protocols
Floating	Perform BC1.2 and HVDCP protocols
Connected to GND via a 900kΩ Resistor	Only perform BC1.2 detection

VBUS PIN

The VBUS pin has multiple functions for the applications. It could be an input power source for the IPR, the discharging path and the monitor pin for protections and disconnection.

VOLTAGE MEASUREMENT

A ADC is connected to the VBUS pin as well, the VBUS voltage is updated periodically in the VBUS MEASUREMENT register. The I²C master can read this register to make further decision.

ANALOG INPUT PINS

After the initialization, the HUSB238A is able to output the status of current connection. When ADDR/ORIENT is floating during initialization, HUSB238A is in GPIO mode. In this mode, the SDA/SNK_VSET, SCL/SNK_ISET pins are repopulated as analog input pins.

SNK_VSET PIN

This pin is used to set the request voltage. This pin is pulled up internally. Connect a resister with 1% tolerance between SNK_VSET and GND to indicate the SNK_VSET_VOLTAGE value as shown in Table 8.

Table 8. SNK_VSET Setting

R_{SNK_VSET} (kΩ)	Preferred Voltage (V)
0	5
3	9
6.04	12
11	15
19.1	20
Open	28 (if EPR_CAP_SNK=0b, then 20)

The RDO voltage of the HUSB238A is determined by the lower value between SNK_VSET and SNK_PDO2_VOLTAGE. SNK_PDO2_VOLTAGE is programmable by internal fuse options and the default value is 20V. The requested voltage value can be changed dynamically with the resistance value change in GPIO mode.

SNK_ISET PIN

This pin is used to set the request current when the HUSB238A connected as a Sink. This pin is pulled up internally. Connect a resister with 1% tolerance between SNK_ISET and GND to indicate the ISET_CURRENT value as shown in Table 9.

Table 9. SNK_ISET Setting

R_{SNK_ISET} (kΩ)	Preferred CURERNT (A)
0	1.25
2.26	1.5
4.02	1.75
6.04	2
8.45	2.25
11.5	2.5
15.8	2.75
21	3
Open	3.25

The RDO current of the HUSB238A is determined by the lower value between ISET_CURRENT and SNK_PDO2_CURRENT. SNK_PDO2_CURRENT is programmable by internal fuse options and the default value is 3.25A. The requested current value can be changed dynamically with the resistance value change in GPIO mode.

DIGITAL PINS

There are two additional digital pins for extended application. The two pins are FLGIN and FAULT/OUT2.

FAULT/OUT2

The FAULT/OUT2 pin is a digital output pin. It can be assigned as several functions selected by OUT2_SEL.

Fault Indication: Output Low in default. The HUSB238A pulls this pin high in several cases:

- There is not any available PDO in Source Capabilities Message to cover the RDO request voltage or current.
- Stays in Fault state.

The Fault Indication is reset after an initialization, SW_RES, change of OUT2_SEL, or Hard Reset command.

ID Indication: This pin indicates connection state.

Table 10. ID Indication Definition

ID Status	Description
Low	Attached as a Source
High-Z	Attached as a Sink or unattached

General Output2: The output state can be control by writing EN_OUT2. I2C master can write the EN_OUT2 bit to change the output state.

Please note that, this digital output pin is Hi-Z during initialization. The output polarity can be changed by FLG_POLARITY.

FLGIN

The FLGIN pin is a digital input pin. It is an input source for interrupt. This interrupt can be set INT_N low if it is not masked. Furthermore, this input signal can be mapped to disable GATE pin immediately by setting EN_FAULTIN bit.

Please note that, this digital output pin is Hi-Z during initialization.

INPUT AND OUTPUT PINS

There are 3 pins that are implemented by dual functions. They are all input and output pins. However, they perform input pin only during initialization when the HUSB238A determines the settings by these pin. After the initialization, these pins switches to output pin with push-pull output. These pins are DBG_N, EN_HVDCP/OUT1 and ADDR/ORIENT.

DEBUG_N PIN

The DEBUG_N pin is a push-pull output that indicate HUSB238A connection status in Table 11:

Table 11. DEBUG_N Pin Definition

DEBUG_N Status	Description
Low	Debug Accessory detected
High	Debug Accessory not detected

ORIENT PIN

The ORIENT pin is a push-pull output that indicate HUSB238A connection status in Table 12.

Table 12. ORIENT Pin Definition

ORIENT Status	Description
Low	STATUS[5:4]=00b,11b or 01b
High	STATUS[5:4]=10b

OUT1 PIN

The OUT1 pin is purely a general output pin, which can be controlled by the EN_OUT1.

CC LOGIC

HUSB238A is able to support the USB Type-C Rev.2.1. CC1 and CC2 pins are used to detect the attachment or detachment with the external devices.

SOP VDM MESSAGES

HUSB238A supports Structured VDMs. Therefore, the Discover Identity, Discover SVIDs, Discover Modes, Enter Mode and Exit Mode Commands are all supported by HUSB238A . HUSB238A can initial Structure VDMs via the GO_COMMAND or respond a received Structure VDM REQ.

POLICY ENGINE

The following sections describes the system policy for typical applications.

SINK REQUESTED POWER DETERMINATION

The request data object (RDO) could be determined in different ways in different modes.

RDO IN GPIO MODE

The HUSB238A can request different voltage per the predetermined settings. There are two ways where the request voltage can be set. One is the configuration of SNK_ISET and SNK_VSET pin and another way is the SNK_RDO2 Configurations. The HUSB238A compares the two values and uses the lower value as its target RDO in GPIO mode.

For example, if the SNK_VSET and SNK_ISET is configured as 9V / 3A. The SNK_RDO2 Configurations is 12V / 2A. Then the RDO that HUSB238A requests from the PD source is 9V / 2A.

After the RDO is determined, the HUSB238A loops through the PD source PDOs from highest voltage first to find the first PDO that satisfies the following conditions:

1. SOURCE_PDO_VOLTAGE ⩽ RDO_VOLTAGE
2. SOURCE_PDO_CURRENT ⩾ RDO_CURRENT

If both the conditions above are satisfied, then HUSB238A sends a request for this source PDO with operating current set to the RDO current value.

If either one of the condition is not satisfied, the HUSB238A continues to compare with the second highest voltage source PDO or requests 5V source PDO directly, depending on the RDO_VOLTAGE_SELECT.

When the actual requested RDO is less than target RDO, the Cap Mismatch bit is sent in the actual requested RDO.

The RDO results are also suitable for legacy charging protocol request. When performing the legacy charging protocol detection, the request voltage is also determined by this RDO results.

RDO IN I²C MODE

Additionally, in I²C mode, HUSB238A can access the internal registers to dynamic change the RDO by I²C bus. After initialization, the HUSB238A may receive the Source Capabilities message from the PD source adapter and the HUSB238A saves the source capability information in registers SRC_PDO_5V to SRC_PDO_20V. The I²C master can visit the HUSB238A registers through the I²C bus and select a proper PDO by setting SRC_PDO register and then writing 0x01 to GO_COMMAND register.

The I²C has the highest priority. If using I²C to select a source PDO, it over writes the internal RDO which is created by SNK_VSET, SNK_ISET pins and internal factory fuse option, and the HUSB238A requests the I²C selected source PDO once the I²C commands are written.

LEGACY CHARGER DETECTION

After the power on reset, the HUSB238A runs the PD PE or Apple Divider 3 and BC1.2 detections simultaneously when PD_PRIOR=1. If PD_PRIOR =0, the PD PE is enabled 3s late after the connection is established.

For BC1.2 detection, the HUSB238A detects SDP (Standard Data Port), CDP (Charging Data Port) and DCP (Dedicated Charging Port) sequentially.

If DCP is detected and HVDCP is enable, the HUSB238A performs HVDCP detection further.

EMARKER EMULATION

The HUSB238A is able to respond a Discover Identity message in SOP' format. No additional analog circuit is needed. The HUSB238A also can be configured to only respond the Discover Identity SOP' message when a PD contract is established. USB238A also ca only responds the Discover Identity SOP' message when a PD contract is established, USB238A also ca only responds the Discover Identity SOP' message when a PD contract is established. This function can be enabled or disabled by internal effuse option.

FAULT RESPONSE

The HUSB238A implements multiple protections to prevent any damage from failure. CCOV, OVP, UV, TSD, UVLO are all involved.

CC OVER VOLTAGE PROTECTION

Since CC1 and CC2 in Type-C connector is very close to VBUS pin, it is possible that the CC1 and CC2 pins are shorted to VBUS pin in some unexpected cases. It is important to guarantee that the CC1 and CC2 pins can be survived under such accidents. When the CC over-voltage condition occurs, the HUSB238A enters fault mode, If the fault is removed, the device enters into unattached mode after 50ms.

OVER VOLTAGE PROTECTION

The HUSB238A detects the VBUS pin voltage to achieve over-voltage protection function. The OVP threshold is changed with the Requested Voltage. When the over-voltage condition occurs, the HUSB238A enters fault Mode, the HUSB238A turns off the external PMOS, the internal 5.1k Rd resistor is also disconnected during fault mode. If the fault is removed, the device enters into unattached mode after 50ms.

The VBUS OV threshold is shown in Table 13.

Table 13. Over-voltage Protection Threshold

Requested Voltage (V)	Over-voltage Threshold
5 V and less	6 V
5 V to 26 V	120% of Requested Voltage
Higher than 26 V	31 V

UNDER VOLTAGE PROTECTION

The HUSB238A detects the VBUS pin voltage to achieve a disconnection detection. When the under voltage fault occurs, the HUSB238A moves out the Attached.SNK state.

Please note that this disconnection detection is only valid when the requested VBUS voltage is higher than 5 V. when the request voltage is equal to 5 V (FPDO=5V, QC2, BC1.2 and Divider 3), the disconnection threshold is vVB_{PRS_F}. If the request RDO is APDO, the UV detection is ignored. Refer to the Table 14.

Table 14. Under-voltage Threshold in Sink Mode

Requested Voltage (V)	Under-voltage Threshold
5 V	vVB_{PRS_F}
5 V to 10 V	80% of Requested Voltage
10 V to 26 V	86% of Requested Voltage
Higher than 26 V	22.4 V

THREMAL SHUT DOWN

The HUSB238A integrates thermal shut down function. It monitors the internal junction temperature. When the junction temperature reaches the thermal shut down threshold T_{TSD_R} for t_{TSW}, and the current requested voltage is higher than 5 V, the HUSB238A requests 5V voltage directly, regardless of the previous established contract, to reduce the total system power. If the junction temperature reaches the thermal shut down threshold T_{TSD_R} for t_{TSD}, the TSD fault can be set to entry the fault mode. If the fault is removed, the device enters into unattached mode after 50ms..

I²C MODE

After the initialization, the HUSB238A is able to output the status of current connection. When ADDR/ORIENT is connected to VDD or GND during initialization, HUSB238A is in I²C mode. In this mode, the INT_N, SDA/SNK_VSET, SCL/SNK_ISET pins are repopulated as I²C interface pins.

INT_N

The INT_N pin is an active LOW open drain interruption output used to prompt the processor to access the I²C registers. An external pull-up resistor is recommended for INT_N pin to output a high voltage level when this pin is not active. The pull-up voltage should be same as the pull-up voltage of SCL and SDA.

SCL AND SDA

The HUSB238A implements a Fast-mode I²C interface. The SCL and SDA pins can detect the status of the input signals and drive the I²C bus when needed.

DEAD BATTERY

The HUSB238A works as PD sink role which requires Rd resistor to be presented on the CC pins even in the un-powered state for successful Type-C detection by source adapter.

The dead battery function supports default USB, 1.5 A and 3.0 A source broadcast Rp current.

SLEEP MODE

The HUSB238A has a specified Sleep Mode to save the power consumption from VDD or VBUS. This function can be enabled or disabled by internal fuse option.

TYPICAL APPLICATION CIRCUITS

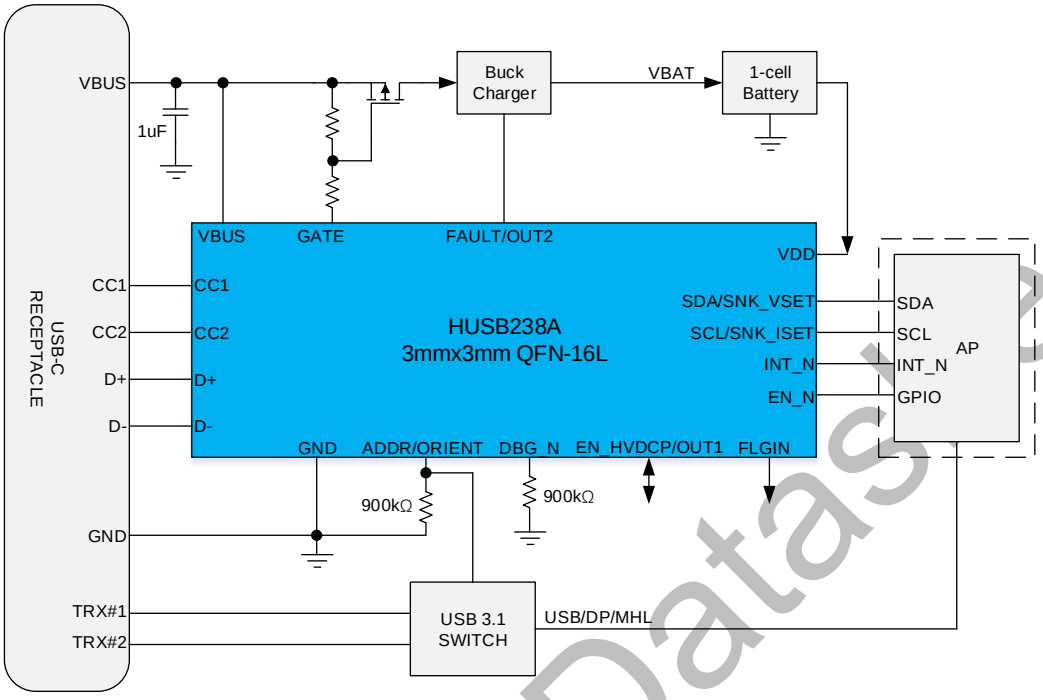


Figure 4. HUSB238A Typical Application in I2C mode

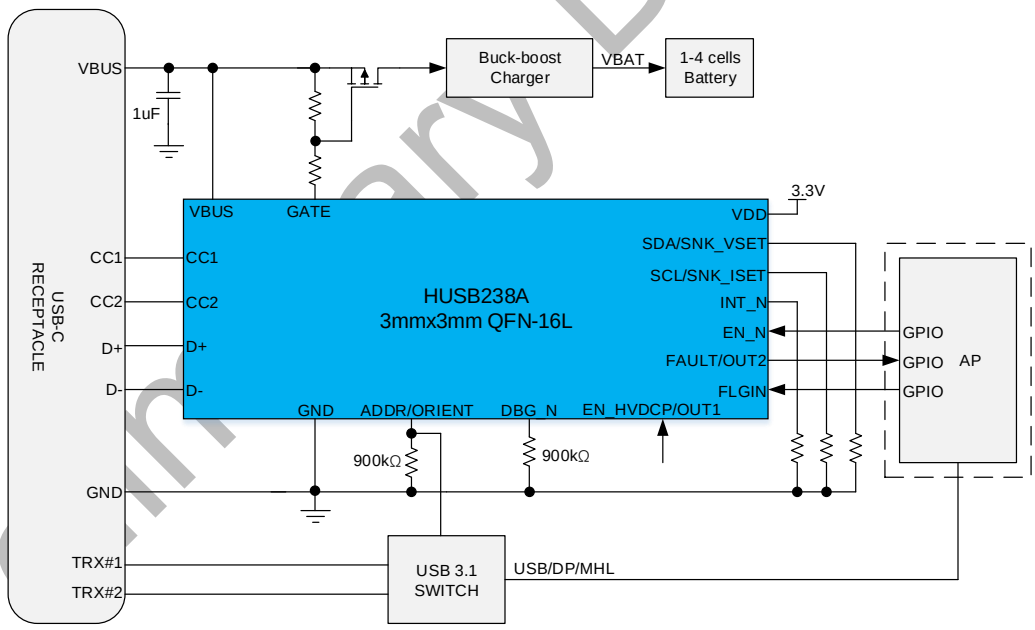
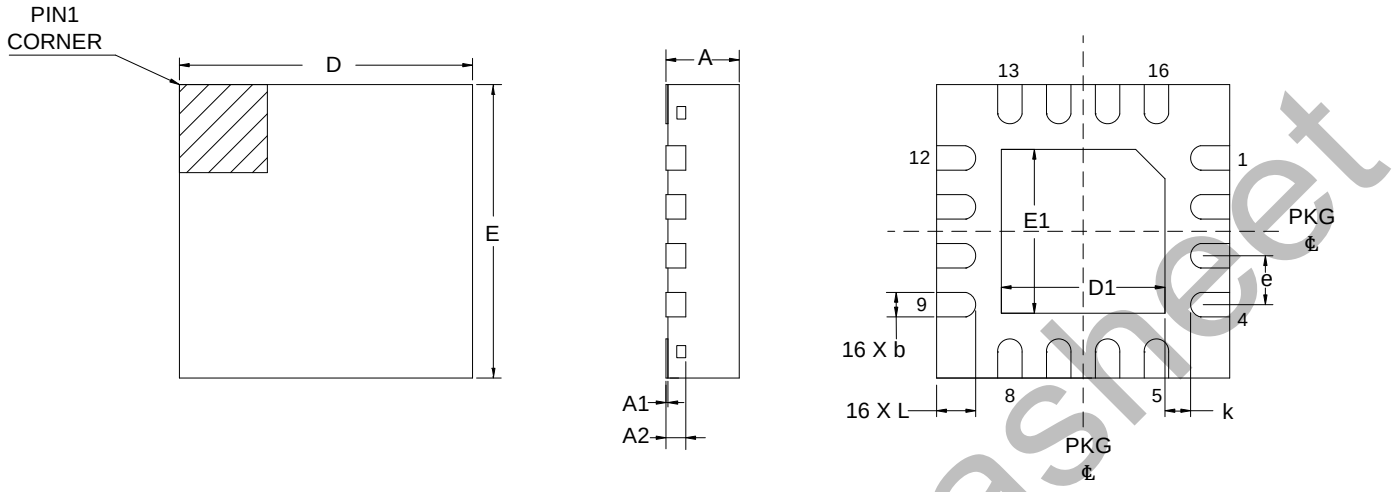


Figure 5. HUSB238A Typical Application in GPIO mode

PACKAGE OUTLINE DIMENSIONS



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOLS	DIMENSION IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
D1	1.55	1.70	1.80
E1	1.55	1.70	1.80
e		0.50 BSC	
L	0.30	0.40	0.50
k		0.20 MIN.	

Figure 6. 3 mm × 3 mm QFN-16L Package

PACKAGE TOP MARKING

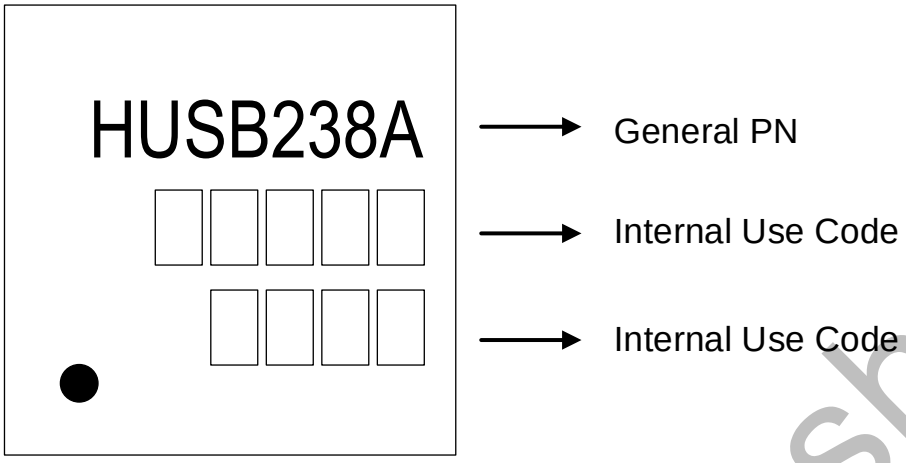


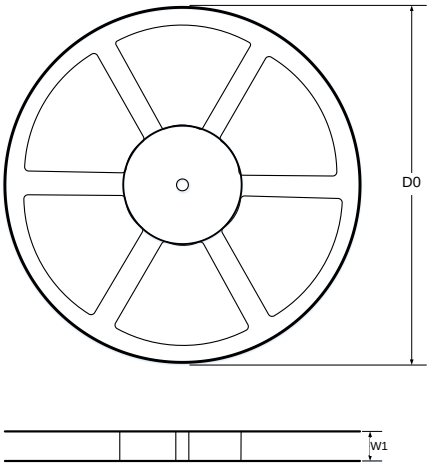
Figure 7. Package Top Marking

ORDERING GUIDE

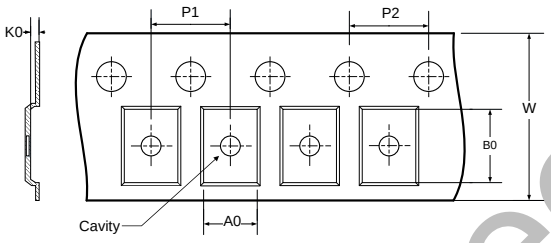
Model	Temperature Range	MSL	Package Option
HUSB238A-AA000-QN16R	-40℃ to 125℃	MSL3	Tape & Reel, 4000

TAPE AND REEL INFORMATION

REEL DIMENSIONS

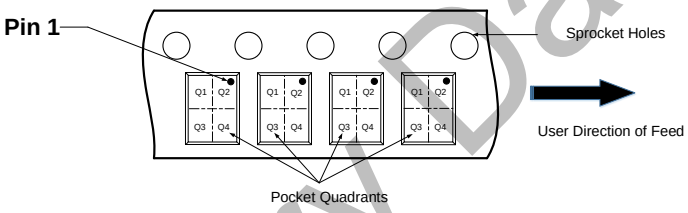


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W： Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

Device	Package Type	D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
HUSB238A-AA000-QN16R	QFN3X3-16L	330.00	12.40	3.35	3.35	1.13	8.00	4.00	12.00	Q2	4000

All dimensions are nominal

Figure 8. Tape and Reel Information

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