USB Type-C Port Controller with I²C and GPIO Control

Hynetek Semiconductor Co., Ltd.

HUSB320

FEATURES

- Fully Autonomous USB Type-C Port Controller
- Support USB Type-C Specification Reversion 2.1
- Source, Sink and DRP Port Role Configuration with Optional Accessary Support
- Try.SRC and Try.Snk Modes for User Configurations
- VDD Operating Range: 2.85 V to 5.5 V
- Multiple IO Voltage Support : 1.2 V, 1.8 V and 3.3 V
- Typical Low Power Operation: I_{VDD_STBY}< 30 μA
- GPIO Mode or Configurable I²C Mode
- Maximum 28 V DC Tolerance on ID, VBUS_DET, CC1 and CC2 Pins
- Dead Battery Support
- 4 kV HBM ESD Rating for USB IO Pins
- Small Package, 12 Lead QFN (1.6 mm x1.6 mm)

APPLICATIONS

Smartphones
Tablets
Accessories
Industrial
Power Banks

GENERAL DESCRIPTION

The HUSB320 is designed for a USB Type-C port. It integrates the CC logic detection and output the connection results per the different connection combinations. The HUSB320 is freely to be configured by user as a Source, Sink or DRP. Additionally, the debug accessories and audio accessories are both supported to be recognized.

The HUSB320 can run in two modes: I²C mode and GPIO mode. In I²C mode, an I²C master can access the HUSB320 to configure the settings or read back status. While in GPIO mode, the configuration is achieved via the pins and the detection results are presented at these pins.

The ultra-low operation current of the HUSB320 helps the system to reduce the total power dissipation and suitable for a battery application.

TYPICAL APPLICATION CIRCUIT

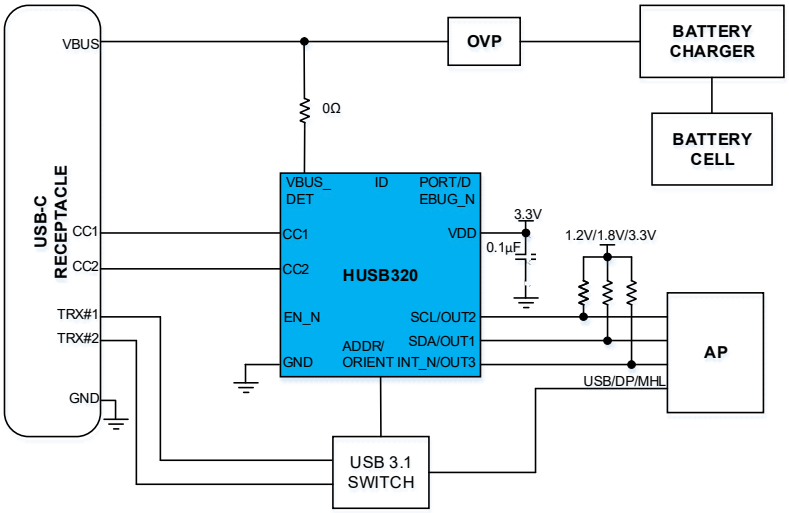


Figure 1. HUSB320-BA000-QN12R Typical Application Circuit

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	11/2022	Initial version
Rev. 1.1	01/2023	Update ORDERING GUIDE (Add Model: HUSB320-BA000-QN12R) Add Table 24. HUSB320-BA000 MASK (Address: 0x0E) Configurations Add Table 31. HUSB320-BA000 USER CFG (Address: 0x16) Configurations
Rev. 1.2	02/2023	Update Typical Application Circuit Update ORDERING GUIDE (Add Model: HUSB320-BA001-QN12R)
Rev. 1.3	04/2023	Add Package Top Marking

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Version	Date	Descriptions
		Update ORDERING GUIDE （Delete Model: HUSB320-AA000-QN12R） Modify the Table Name of MASK Configurations Modify the Table Name of USER CFG Configurations
Rev. 1.4	07/2023	Modify the Typical Application Circuits

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

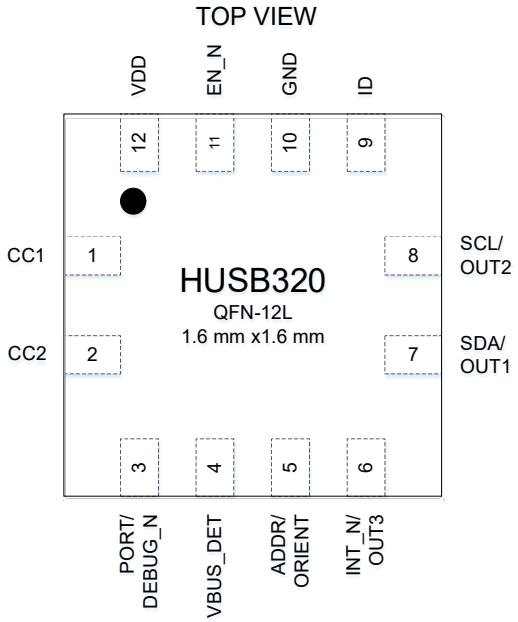


Figure 2. Pin Assignment

Table 1. Pin Function Descriptions

Pin No.	Pin Name	Type[1]	Description
1	CC1	DIO	Type-C configuration channel signal 1
2	CC2	DIO	Type-C configuration channel signal 2
3	PORT/DEBUG_N	IO	Dual function pin. In input mode, this pin (PORT) is a 3 state input to set the port role. The port role is defined as: Connected to VDD via a 900 kΩ resistor = Source Only Connected to GND via a 900 kΩ resistor = Sink Only Float = Dual Role Port (DRP) In output mode, this pin (DEBUG_N) is push-pull output to indicate the Debug Accessory Detection results. Low = Debug Accessory detected High = Debug Accessory not detected
4	VBUS_DET	AI	VBUS voltage detection pin. It could be connected to the VBUS pin at type-C connector or through an 866 kΩ resistor. It is employed for attach and detach detection. It is also the discharge path for VBUS pin when detachment happened
5	ADDR/ORIENT	IO	Dual function pin. In input mode, this pin (ADDR) is a 3 states input to set the working mode. The working mode is defined as: Connected to VDD = I^2C mode with slave address 62H Connected to GND = I^2C mode with slave address 42H Float = GPIO mode Note: a 900 k resistor should be used when connecting to VDD or GND to reduce standby current. In output mode, this pin (ORIENT) is push-pull output to indicate the connection status. Low = CC1 of USB Type-C receptacle is connected High = CC2 of USB Type-C receptacle is connected
6	INT_N/OUT3	IO	Dual functions pin. In I^2C mode, this pin (INT_N) is an open-drain output to request the attention of processor by pulling down this pin.

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Pin No.	Pin Name	Type[1]	Description
			In GPIO mode, this pin (OUT3) is an open-drain output to indicate Audio Accessory detection results: Low = Audio Accessory is detected High-Z = Audio Accessory is not detected
7	SDA/OUT1	IO	Dual functions pin. In I^2C mode, this pin (SDA) is the data line of I^2C bus. In GPIO mode, this pin (OUT1) combined with OUT2 and ID pins to indicate the connection status
8	SCL/OUT2	IO	Dual functions pin. In I^2C mode, this pin (SCL) is the clock line of I^2C bus. In GPIO mode, this pin (OUT2) combined with OUT1 and ID pins to indicate the connection status
9	ID	O	Open-drain output pin. This pin combined is used to indicate the connection status
10	GND	P	Ground connection point
11	EN_N	AI	Chip enabled pin. It is pulled up internally and the HUSB320 is enabled by pulling this pin to GND
12	VDD	P	Input supply for internal circuitry

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

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RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

Parameter	Rating
VDD Input Voltage	2.85 V to 5.5 V
VBUS_DET Input Voltage	4 V to 22 V
Operating Temperature Range (Junction)	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

SPECIFICATIONS

V_{VDD} = 2.85 V to 5.5 V, T_A = 25°C for typical specifications, unless otherwise noted.

Table 3. Electrical Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Power Supply						
VDD UVLO Rising Threshold	$V_{VDD_UVLO_R}$	Power Up to normal operation		2.75	2.9	V
VDD UVLO Hysteresis	$V_{VDD_UVLO_HYS}$	Hysteresis Voltage to shutdown		0.08		V
VDD Leakage Current	$I_{VDD_DISABLE}$	V_{VDD}>$V_{VDD_UVLO_R}$ and EN_N=High or V_{VDD}< $V_{VDD_UVLO_R}$ - $V_{VDD_UVLO_HYS}$			5	μA
VDD Standby Current	I_{VDD_STBY}	EN_H=Low and configured in Sink without attachment, V_{VDD}=4.5 V		15	30	μA
		EN_H=Low and configured in Source or DRP without attachment, V_{VDD}=4.5 V		15	30	μA
VDD Operating Current	I_{VDD_OP}	EN_H=Low and attached as a Sink or Source, V_{VDD}=4.5 V		15	30	μA
Open Drain Output Pins (ID, INT_N/OUT3)						
Output Low Voltage	V_{OL_OD}	Sink current=2 mA			0.4	V
Output Low Resistance	R_{OL_OD}				200	Ω
Input Pin (EN_N)						
Internal Pull Up Resistance	R_{PU_EN}	To VDD pin		6		MΩ
Low Level Input Threshold	V_{IL_EN}				0.4	V
High Level Input Threshold	V_{IH_EN}		0.8			V
Enable Time	t_{EN}	From EN_N=Low to HUSB320 is ready to output stable status or I^2C accessible			100	ms
Input and Output Pins (PORT/DEBUG_N, ADDR/ORIENT)						
Low Level Input Threshold	V_{IL_ADDR}				0.2·V_{VDD}	V
Middle Level Input Threshold	V_{IM_ADDR}		0.44·V_{VDD}		0.56·V_{VDD}	V
High Level Input Threshold	V_{IH_ADDR}		0.8·V_{VDD}			V
Impedance to VDD	Z_{float}	Pins are floating		3.3		MΩ
Output Low Voltage	V_{OL_PP}	Sink current=1 mA			0.2·V_{VDD}	V
Output High Voltage	V_{OH_PP}	Source current=1 mA	0.8·V_{VDD}			V
I^2C Interface Pins (SDA/OUT1, SCL/OUT2)						
SDA/OUT1 Output Low Voltage	V_{OL_OUT1}	Sink current=2 mA			0.3	V
SCL/OUT2 Output Low Voltage	V_{OL_OUT2}	Sink current=2 mA			0.4	V

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Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Low Level Input Threshold	V_{ILI2C_H}	1.8 V and 3.3 V I^2C Bus Voltage Selected			0.4	V
	V_{ILI2C_L}	1.2 V I^2C bus voltage selected			0.4	V
High Level Input Threshold	V_{IHI2C_H}	1.8 V and 3.3 V I^2C bus voltage selected	1.2			V
	V_{IHI2C_L}	1.2 V I^2C bus voltage selected	0.8			V
SDA Pin Leakage Current	I_{LKG_SDA}	SDA/OUT1 pin is High-Z			2	µA
SCL Pin Leakage Current	I_{LKG_SCL}	SCL/OUT2 pin is High-Z			2	µA
Type-C Pins (CC1, CC2)						
Default R_p Current	I_{RP_DEF}	$V_{VDD} \geq 3.5$ V	64	80	96	µA
1.5 A R_p Current	$I_{RP_1.5A}$	$V_{VDD} \geq 3.5$ V	165.6	180	194.4	µA
3 A R_p Current	I_{RP_3A}	$V_{VDD} \geq 3.5$ V	303.6	330	356.4	µA
Dead Battery Clamp Voltage	V_{SNKDB0}	Configured as Sink with 80 µA ±20% R_p Current from Source, V_{VDD}< $V_{VDD_UVLO_R}$	0.25		1.5	V
	V_{SNKDB1}	Configured as Sink with 180 µA ±8% R_p Current from Source, V_{VDD} < $V_{VDD_UVLO_R}$	0.45		1.5	V
	V_{SNKDB2}	Configured as Sink with 330 µA ±8% R_p Current from Source, V_{VDD} < $V_{VDD_UVLO_R}$	0.85		2.18	V
Sink Pull Down Resistor	R_d		4.6	5.1	5.6	kΩ
CC Impedance	z_{OPEN}	CC1 or CC2 are disabled from applying R_p or R_d	1000			kΩ
R_a Detection Threshold as Source	vR_{a_SRCDEF}	Configured as Source with I_{RP_DEF}	0.15	0.2	0.25	V
	$vR_{a_SRC1.5A}$	Configured as Source with $I_{RP_1.5A}$	0.35	0.4	0.45	V
	vR_{a_SRC3A}	Configured as Source with I_{RP_3A}	0.75	0.8	0.85	V
R_d Detection Threshold as Source	vR_{d_SRCDEF}	Configured as Source with I_{RP_DEF}	1.55	1.6	1.65	V
	$vR_{d_SRC1.5A}$	Configured as Source with $I_{RP_1.5A}$	1.55	1.6	1.65	V
	vR_{d_SRC3A}	Configured as Source with I_{RP_3A}	2.45	2.6	2.75	V
R_a Detection Threshold as Sink	vR_{a_SNK}	Configured as Sink	0.15	0.2	0.25	V
R_d Detection Threshold as Sink	vR_{d_SNKDEF}	Configured as Sink with I_{RP_DEF} attached	0.61	0.66	0.7	V
	$vR_{d_SNK1.5A}$	Configured as Sink with $I_{RP_1.5A}$ attached	1.16	1.23	1.31	V
	vR_{d_SNK3A}	Configured as Sink with I_{RP_3A} attached	2.04	2.11	2.18	V
VBUS Present Rising Threshold	vVB_{PRS_R}	Rising edge to set VBUSOK=1b	3.67	4	4.4	V
VBUS Present Hysteresis	vVB_{PRS_HYS}	Hysteresis voltage to set VBUSOK=0b		0.7		V
VBUS Present Debounce	t_{DEB_VB}	Debounce time for valid VBUSOK flag	250	375	500	µs
vSafe0V Falling Threshold	v_{Safe0V_F}	Falling edge to set vSafe0V=1b		0.8		V
vSafe0V Hysteresis	v_{Safe0V_HYS}	Hysteresis Voltage to set vSafe0V=0b		20		mV
vSafe0V Debounce	$t_{DEB_vSafe0V}$	Debounce time for valid VBUSOK flag	250	375	500	µs
VBUS_DET Discharge Resistance	R_{DSCHG_VB}	VBUS_DET to GND path resistance when detachment event happens		2		kΩ
AUTOSNK Threshold	$v_{AUTOSNKth0}$	CONTROL1[6:5]=00b	2.9	3.0	3.1	V
	$v_{AUTOSNKth1}$	CONTROL1[6:5]=01b	3.0	3.1	3.2	V
	$v_{AUTOSNKth2}$	CONTROL1[6:5]=10b	3.1	3.2	3.3	V
	$v_{AUTOSNKth3}$	CONTROL1[6:5]=11b	3.2	3.3	3.4	V

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Table 4. Timing Parameters

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Global Timing						
Input Lock Time	t_{IOLOCK}	Time for input and output pins to sample input signal		10		ms
Soft Reset Duration	t_{RESET}	From Soft Reset is executed to HUSB320 is ready to output stable status or I^2C accessible			100	ms
AUTOSNK Debounce Time	$t_{AUTOSNK}$	Debounce time for entering or exiting AUTOSNK mode if it is enabled		15		ms
Enable Time	t_{EN}	From EN_N=Low to HUSB320 is ready to output stable status or I^2C accessible			100	ms
Type-C Timing						
CC Attach Debounce Time	$t_{CCDebounce0}$	CONTROL1[2:0]=011b		150		ms
WaitSink Debounce Time for Detach	$t_{PDDebounce}$		10	15	20	ms
AttachedSink Debounce Time for Detach	$t_{SinkDisconnect2}$			0		ms
Wait time for Attach in Try Action	$t_{TryCCDebounce}$		10		20	ms
Sink Detection Time for R_p Change	$t_{RpValueChange}$	USER_CFG[1:0]=10b	10		20	ms
Source Debounce Time for Detach	$t_{SRCDisconnect}$				20	ms
Error Recovery Duration	$t_{ErrorRecovery}$		25	50	100	ms
Toggling Period	t_{DRP1}	CONTROL[7:6]=01b		70		ms
SNK Duration in DRP Toggling	$t_{DRPtogSNK0}$	CONTROL[5:4]=00b, Refer to t_{DRP}		60		%
SRC Duration in DRP Toggling	$t_{DRPtogSRC0}$	CONTROL[5:4]=00b, Refer to t_{DRP}		40		%
I^2C Timing						
SCL/OUT2 Clock Frequency	f_{SCL}		50		400	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.6			μs
Low Period of SCL/OUT2 Clock	t_{LOW}		1.3			μs
High Period of SCL/OUT2 Clock	t_{HIGH}		0.6			μs
Set−up Time for Repeated START Condition	$t_{SU;STA}$		0.6			μs
Data Hold Time	$t_{HD;DAT}$		0			μs
Data Set−up Time	$t_{SU;DAT}$		100			ns
Rise Time of SDA/OUT1 and SCL/OUT2 Signals	t_r				250	ns
Fall Time of SDA/OUT1 and SCL/OUT2 Signals	t_f				250	ns
Set−up Time for STOP Condition	$t_{SU;STO}$		0.6			μs
Bus−Free Time between STOP and START Conditions	t_{BUF}		1.3			μs
Data Valid Time	$t_{VD:DAT}$				0.9	μs
Data Valid Acknowledge Time	$t_{VD:ACK}$				0.9	μs
Pulse Width of Spikes that Must Be Suppressed by the Input Filter	t_{SP}				50	ns

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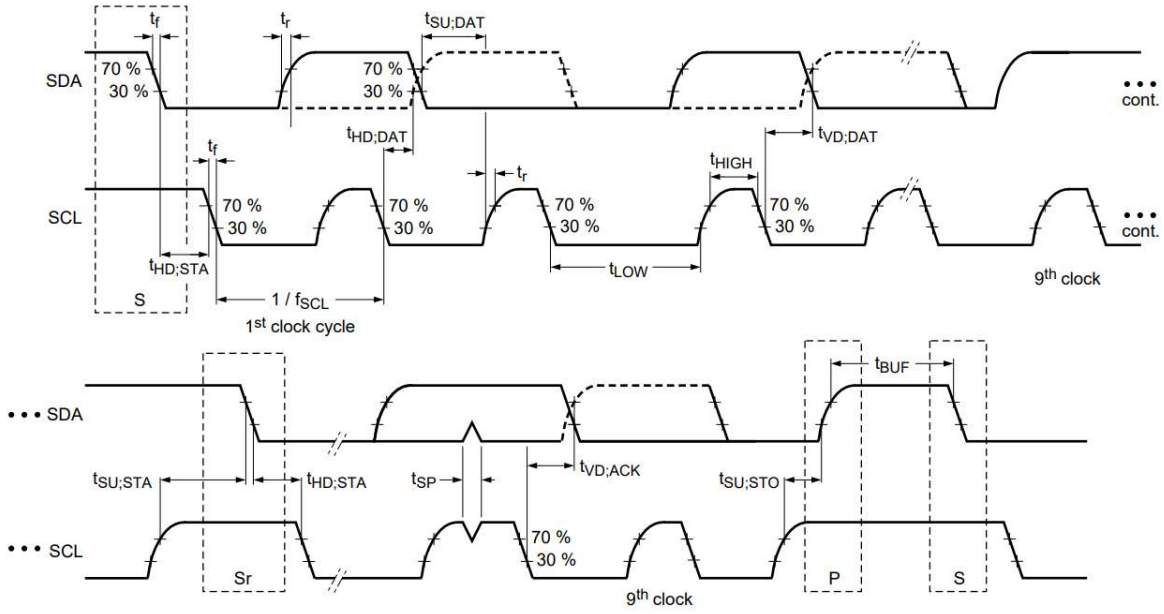


Figure 3. I²C Timing

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ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
VDD, PORT/DEBUG_N, ADDR/ORIENT, EN_N, INT_N/OUT3 Pins	-0.3 V to 6.5 V
CC1, CC2, VBUS_DET, ID Pins	-0.3 V to 28 V
SDA/OUT1, SCL/OUT2 Pins	-0.3 V to 6.5 V
Operating Temperature Range (Junction)	−40°C to 125°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model (CC1, CC2, VBUS_DET Pins)	±4000 V
Human Body Model (Other Pins)	±2000 V
Charged Device Model	±500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
QFN1.6x1.6-12L	164.4	47.1	°C/W

ESD CAUTION



Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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FUNCTIONAL BLOCK DIAGRAM

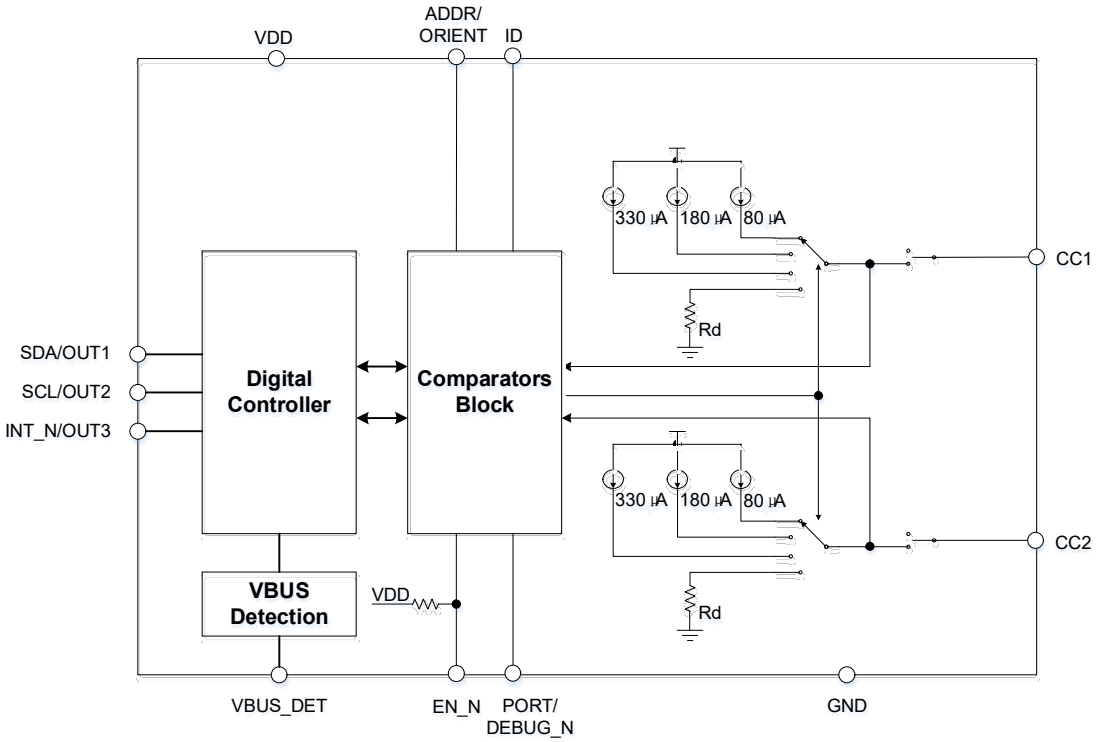


Figure 4. HUSB320 Functional Block Diagram

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THEORY OF OPERATION

The HUSB320 is a CC logic controller, which can support most of the Type-C functions. It integrates all of necessary function blocks which are necessary in Type-C mode. Besides the typical Type-C roles functions including Source, Sink and DRP, the HUSB320 also supports to detect a Type-C port with accessories. It can also configured as Source preferred with Try.SRC function or Sink preferred with Try.Sink function. All of functions are configurable via the I²C interface.

ENABLE CONTROL

The HUSB320 has an enable pin (EN_N) for the whole system control. This pin is pulled up by R_{PU_EN} internally. There is an input comparator implemented for this input voltage. This output of this comparator is going to enable the whole system control.

VDD AND INITIALIZATION

The HUSB320 is powered by VDD pin. It has an internal UVLO for its power input VDD voltage (V_{VDD}). When V_{VDD} is lower than $V_{VDD_UVLO_R}$, all of pins are in HIZ mode (not include CC pins configured as Sink or DRP). With the increase of VDD voltage to exceed the $V_{VDD_UVLO_R}$, the HUSB320 start initialization.

DOWNLOAD

With the ready status of VDD and the HUSB320 is enabled, the digital core start to download the trim values and default settings for the internal memory and registers. Only when download is completed, the HUSB320 starts to configure the blocks by the download values.

INITIALIZATION

After the download, the HUSB320 enables initialization. The input function of input and output pins (PORT/DEBUG_N and ADDR/ORIENT pins) is selected during this initialization process. The HUSB320 samples the input status of these pins in t_{IOLOCK} and updates the I²C address or port role configuration register. Then the HUSB320 switches these pin to output status. After the I²C accessibility is ready, the HUSB320 is ready to run normal operation and the initialization is done.

During initialization, PORT/DEBUG_N is an input pin for determining the role of the HUSB320. With different connections, the role of the HUSB320 is set as Table 7.

Table 7. Port Role Configuration

PORT/DEBUG_N Connection	HUSB320 Role Configured
Connected to VDD via a 900 kΩ Resistor	Source only
Floating	DRP
Connected to GND via a 900 kΩ Resistor	Sink only

With the sampled status of PORT/DEBUG_N pin, the role settings are updated at Register PORTROLE[2:0]. Please note that, the Port Role of the HUSB320 may be not fixed after the initialization. The I²C master may access the PORTROLE register to re-configure the PORTROLE during normal operation.

For ADDR/ORIENT pin, it is employed to select whether the HUSB320 works as I²C mode or GPIO mode. As shown in Table 8 :

Table 8. Work Mode Configuration

ADDR/ORIENT Connection	HUSB320 Role Configured
Connected to VDD via a 900 kΩ Resistor	I²C mode with slave address=62H
Floating	GPIO mode
Connected to GND via a 900 kΩ Resistor	I²C mode with slave address=42H

As shown in Table 8, when worked in I²C mode, the salve address of the HUSB320 is as below:

Table 9. I2C Slave Address

Bit	7	6	5	4	3	2	1	0
Value	0	1	ADDR/ORIENT	0	0	0	1	R/W

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POWER OFF

If the VDD falls under ($V_{VDD_UVLO_R}$-$V_{VDD_UVLO_HYS}$) any time, all of the internal circuit would be reset and wait for the next rising of VDD.

VBUS_DET PIN

The VBUS_DET pin has two configurations for different applications.

When configurations VBUS_DET pin External resistor 0 Ω ,The VBUS_DET pin is employed to sense the VBUS pin of USB type-C port. It can indicate the VBUS voltage status per two signals. The signals of VBUSOK and vSafe0V are sent to digital block to help determine the attach or detach status.

Beside, VBUS_DET pin has implemented an internal discharge resistor to dissipate the energy stored in the VBUS capacitors when needed.

When configurations VBUS_DET pin External resistor 866 kΩ , the VBUS_DET pin is designed to have an external resistor in series when connected to the VBUS pin at type-C connector. The VBUS voltage is divided externally and then sensed by the VBUS_DET pin to perform the VBUS_OK detection only. The VBUS_OK signal is sent to digital block to help determine the attach or detach status.

Please note that the SAFE_0V_DET detection and VBUS discharger is not enabled when configurations VBUS_DET pin External resistor 866 kΩ . The SAFE_0V_DET is forced to be always 1.

GPIO PINS

After the initialization, the HUSB320 is able to output the status of current connection. When ADDR/ORIENT is floating during initialization, the HUSB320 is in GPIO mode. In this mode, the INT_N/OUT3, SDA/OUT1, SCL/OUT2 pins are repopulated as output pins.

OUT3

The OUT3 pin is an open drain output pin, which indicates the Audio Accessory detection results in Table 10:

Table 10. OUT3 Pin Definition

OUT3 Status	Description
Low	HUSB320 enters AudioAccessory State
High-Z	HUSB320 is not in AudioAccessory State

OUT2 AND OUT1

The OUT2 and OUT1 pin are combined to indicate the attached status in Table 10 and Table 10:

Table 11. OUT1 and OUT2 Pin Definition when Enable the ADDR and PORT pin output mode

ID Status	OUT1 Status	OUT2 Status	Description
High-Z	High-Z	Low	Unattached
High-Z	High-Z	High-Z	SNK with Default R_p
High-Z	Low	High-Z	SNK with 1.5A R_p
High-Z	Low	Low	SNK with 3A R_p
Low	High-Z	High-Z	SRC with Default R_p
Low	Low	High-Z	SRC with 1.5A R_p
Low	Low	Low	SRC with 3A R_p
Low	High-Z	Low	Reserved

Table 12. OUT1 and OUT2 Pin Definition when Disable the ADDR and PORT pin output mode

ID Status	OUT1 Status	OUT2 Status	Description
High-Z	High-Z	High-Z	Unattached
High-Z	High-Z	Low	SNK with Default R_p
High-Z	Low	High-Z	SNK with 1.5A R_p
High-Z	Low	Low	SNK with 3A R_p
Low	High-Z	Low	SRC with Default R_p

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ID Status	OUT1 Status	OUT2 Status	Description
Low	Low	High-Z	SRC with 1.5A R_p
Low	Low	Low	SRC with 3A R_p
Low	High-Z	High-Z	Reserved

ID PIN

The ID pin is an open drain output that indicate the HUSB320 connection status in Table 10:

Table 13. ID Pin Definition

ID Status	Description
Low	Attached as a Source
High-Z	Attached as a Sink or unattached

DEBUG_N PIN

The DEBUG_N pin is a push-pull output that indicate the HUSB320 connection status in Table 10:

Table 14. DEBUG_N Pin Definition

DEBUG_N Status	Description
Low	Debug Accessory detected
High	Debug Accessory not detected

ORIENT PIN

The ORIENT pin is a push-pull output that indicate the HUSB320 connection status in Table 15.

Table 15. ORIENT Pin Definition

ORIENT Status	Description
Low	STATUS[5:4]=00b,11b or 01b
High	STATUS[5:4]=10b

I²C MODE

After the initialization, the HUSB320 is able to output the status of current connection. When ADDR/ORIENT is connected to VDD or GND during initialization, the HUSB320 is in I²C mode. In this mode, the INT_N/OUT3, SDA/OUT1, SCL/OUT2 pins are repopulated as I²C interface pins.

INT_N

The INT_N pin is an active LOW open drain interruption output used to prompt the processor to access the I²C registers. The detailed Register info is listed in the Register section. An external pull up resistor is recommended for INT_N pin to output a high voltage level when this pin is not active. The pull up voltage should be same as the pull up voltage of SCL and SDA.

SCL AND SDA

The HUSB320 implements a standard I²C interface. The writing and reading action is defined as below.



Figure 5. I²C Write Action

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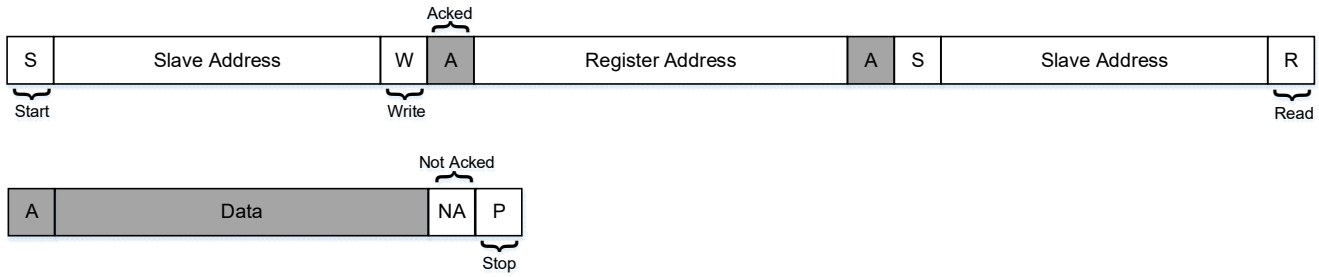


Figure 6. I²C Read Action

The HUSB320 supports the pull up voltage of I²C bus as low as 1.2 V. The HUSB320 divides the pull up voltage into two groups, one is 1.8 V to 3.3 V while another one is 1.2 V.

DEAD BATTERY

DB STATE

When the VDD voltage is lower than $V_{VDD_UVLO_R}$, the HUSB320 supports the dead battery features on both CC1 and CC2 pins. In DB State, The CC1 and CC2 pin is clamped to be lower than V_{SNKDB} when there is an R_p connected to CC1 or CC2 pins (R_d/R_d). There is not any other function enabled expect the EN_N detection.

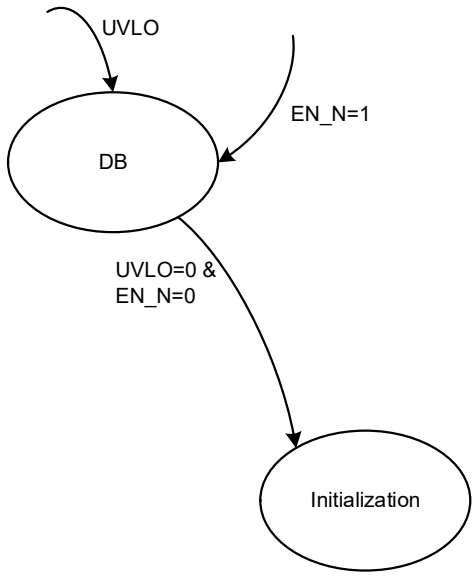


Figure 7. Dead Battery Timing

CC LOGIC

The HUSB320 is able to support the USB Type-C Rev.2.1. It integrates the necessary function blocks for all of Type-C operations. CC1 and CC2 pins are used to detect the attachment/detachment with the external devices.

With different configurations, the HUSB320 is possible connected with different terminations. These possible termination could be R_p current source when the HUSB320 is configured as a Sink, R_d when the HUSB320 is configured as a Source or R_a in a eMarker cable or accessory.

The valid Ra, Rd or R_p are defined as below:

Table 16. Possible Connected External Terminations

External Termination	Min	Typ	Max	Unit
R_a	0.8	1	1.2	kΩ
R_d	4.6	5.1	5.6	kΩ
Default R_p Current Source	64	80	96	μA

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External Termination	Min	Typ	Max	Unit
Resistor to 3.3 V	28.8	36	43.2	kΩ
Resistor to 5 V	44.8	56	67.2	kΩ
1.5 A R_p Current Source	166	180	194	μA
Resistor to 3.3 V	11.4	12	12.6	kΩ
Resistor to 5 V	20.9	22	23.1	kΩ
3 A R_p Current Source	304	330	356	μA
Resistor to 3.3 V	4.46	4.7	4.93	kΩ
Resistor to 5 V	9.5	10	10.5	kΩ

AUTOSNK FUNCTION

The HUSB320 monitors the VDD voltage. There is an internal comparator connected to VDD pin and if the VDD voltage is lower than AUTOSNK_TH, the AUTOSNK function is activated if CONTROL1[4]=1b. AUTOSNK_TH is selected by CONTROL1[6:5].

With the AUTOSNK function, the HUSB320 sets PORTROLE[2:0]=010b to trigger the port role transition. The previous PORTROLE[2:0] is stored. If VDD voltage rises back to be higher than AUTOSNK_TH, AUTOSNK function is deactivated and the PORTROLE[2:0] is resumed to be the previous value.

If CONTROL1[4]=0b, the AUTOSNK function cannot be activated always.

MANUAL FUNCTION

The HUSB320 implements the MANUAL register to provide a way for user to perform some actions. In I^2C mode, It is possible that the MANUAL register is executed.

By writing any bit of MANUAL[3:0] to 1b, the HUSB320 transitions to the correct State per the bit. For MANUAL[3], the target State is Unattached.SNK. If PORTROLE[2:0]=100b or 010b, writing 1b to MANUAL[3] pushes the state back to Unattached.SNK. If PORTROLE[2:0]=001b, this action is ignored.

For MANUAL[2], the target State is Unattached.SRC. If PORTROLE[2:0]=100b or 001b, writing 1b to MANUAL[2] pushes the state back to Unattached.SRC. If PORTROLE[2:0]=010b, this action is ignored.

For MANUAL[1], the target State is Disabled State. Writing 1b to MANUAL[1] pushes the state back to Disabled State. Only writing 0b to MANUAL[1] can exit the Disabled State.

For MANUAL[0], the target State is ErrorRecovery State. Writing 1b to MANUAL[0] pushes the state back to ErrorRecovery State.

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REGISTERS

The HUSB320 has multiple internal registers controlling the function blocks. After the download, all of registers are reset to default values. These registers configure all of the function blocks.

The DEVICE ID register is defined to store the chip info.

Table 17. DEVICE ID (Address: 0x01)

Bit	Field	Type	Description	Default
[7:4]	VER_ID	R	Device version ID	1H
[3:0]	REV_ID	R	Device Revision ID	0H

The DEVICE TYPE register is defined to store the chip info.

Table 18. DEVICE TYPE (Address: 0x02)

Bit	Field	Type	Description	Default
[7:0]	DEVICE_TYPE	R	Device Type ID	03H

The PORTROLE register is the configuration register for Port Role. These bits can be re-written by I²C interface in I²C mode. In this case, any change of Port Role will trigger a transition to ErrorRecovery state. When the last 3 bits are written by multiple 1s. The higher bit has higher priority; the rest bit has no effect on the less priority bits. For instance, the I²C master writes 111b to the bit[2:0]. Only the bit[2] is written successfully and the returned value of bit[2:0] is 100b.

Table 19. PORTROLE (Address: 0x03)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W	Reserved	0b
[6]	ORIENTDEB	R/W	1b: When a Debug Accessory is detected, continue to orientation detection 0b: When a Debug Accessory is detected, do not perform orientation detection	1b
[5:4]	TRY	R/W	Enable control for try mechanism: 00b: Disabled 01b: Try.SNK supported 10b: Try.SRC supported 11b: Disabled	00b
[3]	AUDIOACC	R/W	1b: Enabled Audio Accessory Support 0b: Disable Audio Accessory Support	1b
[2]	DRP	R/W	This bit is updated after initialization automatically. It can be configured via I2C during normal operation. 1b: Configured as DRP 0b: Configured as NOT DRP	PORT/DEBUG_N
[1]	SNK	R/W	This bit is updated after initialization automatically. It can be configured via I²C during normal operation. 1b: Configured as Sink 0b: Configured as NOT Sink	PORT/DEBUG_N
[0]	SRC	R/W	This bit is updated after initialization automatically. It can be configured via I²C during normal operation. 1b: Configured as Source 0b: Configured as NOT Source	PORT/DEBUG_N

The CONTROL register controls the type-C timing parameters. When the HUSB320 is in DRP mode, the CC lines toggles before there is any device attached. The toggling timing is shown in Figure 8

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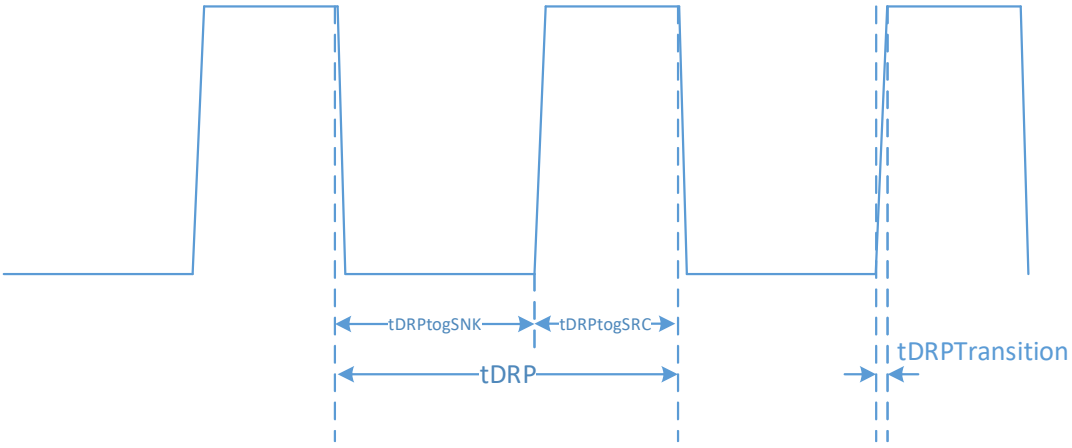


Figure 8. DRP Toggling Timing

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Table 20. CONTROL (Address: 0x04)

Bit	Field	Type	Description	Default
[7:6]	T_DRP	R/W	DRP toggling cycle t_{DRP} 00b: 60 ms 01b: 70 ms 10b: 80 ms 11b: 90 ms	01b
[5:4]	DRPTOGGLE	R/W	Select the toggle duty ($t_{DRPtogSNK}/t_{DRP}$ or $t_{DRPtogSRC}/t_{DRP}$) in DRP toggling: 00b: 60% SNK + 40% SRC 01b: 50% SNK + 50% SRC 10b: 40% SNK + 60% SRC 11b: 30% SNK + 70% SRC	00b
[3]	Reserved	R/W	Reserved	0b
[2:1]	HOST_CUR	R/W	These bits control the R_p current source when configured as Source. 00b: Reserved 01b: 80 µA, Default R_p 10b: 180 µA, 1.5 A R_p 11b: 330 µA, 3 A R_p	00b
[0]	INT_MASK	R/W	This bit is the global interruption mask for all of interruptions. 1b: Mask all of interruptions 0b: Mask is controlled by MASK and MASK1 registers	1b

The CONTROL1 register controls the HUSB320 operation parameters. The debounce timing for a valid detachment is shown in Figure 8

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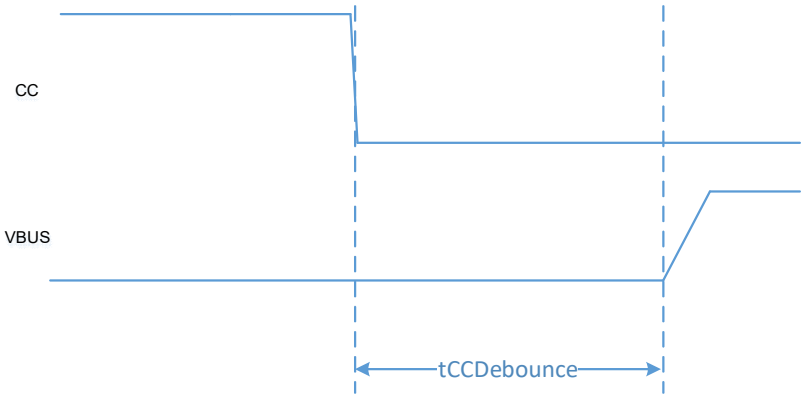


Figure 9. tCCDebuounce Timing

Table 21. CONTROL1 (Address: 0x05)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W	Reserved	0b
[6:5]	AUTO_SNK_TH	R/W	Weak VDD voltage threshold to enable AUTOSNK function. 00b: 3.0 V 01b: 3.1 V 10b: 3.2 V 11b: 3.3 V	01b
[4]	AUTO_SNK_EN	R/W	AUTOSNK function control: Set PORTROLE[2:0]=010b and store the previous value when VDD voltage is lower than AUTO_SNK_TH and back to previous value when VDD voltage is higher than AUTO_SNK_TH 1b: Enabled 0b: Disabled	0b
[3]	ENABLE	R/W	This bit is only valid when HUSB320 is in I²C mode. It can be configured via I²C during normal operation. When I²C mode, writing 0b to this bit push the main state machine to I²CDisable State 1b: Enable the HUSB320 in I²C mode 0b: Disable the HUSB320 in I²C mode	0b
[2:0]	TCCDEB	R/W	Debounce time for attaching a device. 000b: 120 ms 001b: 130 ms 010b: 140 ms 011b: 150 ms 100b: 160 ms 101b: 170 ms 110b: 180 ms 111b: Reserved	011b

The MANUAL register can force the HUSB320 switching to the type-C state per the configuration bit. Only bit[1] in this register is R/W which controlled freely by I²C master. The rest bits are all write one self-clearing (WC), that is these bits can be written 1b by I²C master but will clear to 0b after the execution. When these bits are written by multiple 1b, the bit[1] has the highest priority. The write action of other bits should be ignore. While for the rest bits, the priority is ERROR_REC>FORCE_SRC>FORCE_SNK>UNATT_SRC>UNATT_SNK. For instance, the I²C master writes 0xFF to this register. Only the bit[1] is written successfully and the returned value is 0x02. If the I²C master writes 0xF0 to this register, the bit of FORCE_SRC has high priority and is written successfully. The HUSB320 may start Force Function. Then, the returned value is 0x00.

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Table 22. MANUAL (Address: 0x09)

Bit	Field	Type	Description	Default
[7:6]	Reserved	R/W		00b
[5]	FORCE_SRC	WC	1b: Change PORTROLE[2:0] to 001b temporary if it is not CC1|CC2=R_p in current State 0b: No any action	0b
[4]	FORCE_SNK	WC	1b: Change PORTROLE[2:0] to 010b temporary if it is not CC1|CC2=R_d in current State 0b: No any action	0b
[3]	UNATT_SNK	WC	1b: Jump to Unattached.SNK state forcedly 0b: No any action	0b
[2]	UNATT_SRC	WC	1b: Jump to Unattached.SRC state forcedly 0b: No any action	0b
[1]	DISABLED	R/W	1b: Jump to Disabled state forcedly 0b: Exit Disabled state and enter ErrorRecovery state	0b
[0]	ERROR_REC	WC	1b: Jump to ErrorRecovery state forcedly 0b: No any action	0b

The RESET register is only a command register to execute a reset action for HUSB320. When a write action of 1b to this RESET[0], HUSB320 jumps to initialization state. After the reset action, the return value of this register bit[0] is 0b.

Table 23. RESET (Address: 0x0A)

Bit	Field	Type	Description	Default
[7:6]	Reserved	R/W		00b
[5]	Reserved	R/W		1b
[4]	EN_TOGGLE_DUTY	R/W	Enable control of toggle duty 0b: tDRPToggleSNK and tDRPToggleSRC are configured by CONTROL[5:4] 1b: tDRPToggleSNK and tDRPToggleSRC are changed every 500ms	0b
[3:1]	tDRPTry	R/W	tDRPTry timer settings 000b: 145 ms 001b: 130 ms 010b: 120 ms 011b: 110 ms 100b: 100 ms 101b: 90 ms 110b: 85 ms 111b: 80 ms	000b
[0]	SW_RES	WC	Chip reset. Return to Initialization State 1b: Jump to Initialization state forcedly 0b: No any action	0b

The MASK and MASK1 registers are control registers which set which interruption can set the INT_N pin low to request the I²C master's attention. Please note that, even an interruption is masked in the MASK and MASK1 registers, this interruption bit in INTERRUPT and INTERRUPT1 registers is also set.

Table 24. HUSB320-BAXXX MASK (Address: 0x0E)

Bit	Field	Type	Description	Default
[7]	Reserved	R/W	Reserved	0b
[6]	M_ORIENT	R/W	1b: Mask the I_ORIENT interruption to assert INT_N pin 0b: DO NOT mask the I_ORIENT interruption to assert INT_N pin	0b
[5]	M_FAULT	R/W	1b: Mask the I_FAULT interruption to assert INT_N pin 0b: DO NOT mask the I_FAULT interruption to assert INT_N pin	0b

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Bit	Field	Type	Description	Default
[4]	M_VBUS_CHG	R/W	1b: Mask the I_VBUS interruption to assert INT_N pin 0b: DO NOT mask the I_VBUS interruption to assert INT_N pin	0b
[3]	M_AUTOSNK	R/W	1b: Mask the I_ AUTOSNK interruption to assert INT_N pin 0b: DO NOT mask the I_ AUTOSNK interruption to assert INT_N pin	0b
[2]	M_BC_LVL	R/W	1b: Mask the I_ BC_LVL interruption to assert INT_N pin 0b: DO NOT mask the I_BC_LVL interruption to assert INT_N pin	0b
[1]	M_DETACH	R/W	1b: Mask the I_ DETACH interruption to assert INT_N pin 0b: DO NOT mask the I_ DETACH interruption to assert INT_N pin	0b
[0]	M_ATTACH	R/W	1b: Mask the I_ ATTACH interruption to assert INT_N pin 0b: DO NOT mask the I_ ATTACH interruption to assert INT_N pin	0b

Table 25. MASK1 (Address: 0x0F)

Bit	Field	Type	Description	Default
[7:3]	Reserved	R/W	Reserved	00000b
[2]	M_FRC_FAIL	R/W	1b: Mask the I_FRC_FAIL interruption to assert INT_N pin 0b: DO NOT mask the I_FRC_FAIL interruption to assert INT_N pin	0b
[1]	M_FRC_SUCC	R/W	1b: Mask the I_ FRC_SUCC interruption to assert INT_N pin 0b: DO NOT mask the I_ FRC_SUCC interruption to assert INT_N pin	0b
[0]	Reserved	R/W	Reserved	0b

The STATUS register is read-only register that shows the status of functions.

Table 26. STATUS (Address: 0x11)

Bit	Field	Type	Description	Default
[7]	AUTOSNK	R	1b: AUTOSNK mode is activated (V_{VDD}>AUTO_SNK_TH or AUTO_SNK_EN=0b) 0b: AUTOSNK mode is not activated	0b
[6]	VSAFE0V	R	1b: VBUS is within vSafe0V 0b: VBUS is NOT within vSafe0V	0b
[5:4]	ORIENT	R	CC connection status, Refer to ORIENT Pin section 00b: No SRC.Rd or SNK.Rp or Orient detected 01b: CC1 is within SNK.Rp or SRC.Rd 10b: CC2 is within SNK.Rp or SRC.Rd 11b: Reserved	00b
[3]	VBUSOK	R	1b: VBUSOK is set as 1b 0b: VBUSOK is 0b	0b
[2:1]	BC_LVL	R	In Attached.SNK State, Connected CC line voltage level status. 00b: (R_a or unattached) Sink or unattached Source 01b: Source with default current advertisement 10b: Source with 1.5 A current advertisement 11b: Source with 3 A current advertisement	00b
[0]	ATTACH	R	1b: In the Attached.SRC/Attached.SNK/ DebugAccessory.SNK/ AudioAccessory/UnorientedDebugAccessory.SRC/ OrientedDebugAccessory.SRC states 0b: DO NOT in the Attached.SRC/Attached.SNK/ DebugAccessory.SNK/ AudioAccessory/UnorientedDebugAccessory.SRC/ OrientedDebugAccessory.SRC states	0b

The TYPE register indicates the connection results.

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Table 27. TYPE (Address: 0x13)

Bit	Field	Type	Description	Default
[7]	Reserved	R	Reserved	0b
[6]	DEBUGSRC	R	1b: In the states of Unoriented/Oriented DebugAccessory.SRC 0b: NOT in the states of Unoriented/Oriented DebugAccessory.SRC	0b
[5]	DEBUGSNK	R	1b: In the states of DebugAccessory.SNK 0b: NOT in the states of DebugAccessory.SNK	0b
[4]	SINK	R	1b: In the states of Attached.SNK 0b: NOT in the states of Attached.SNK	0b
[3]	SOURCE	R	1b: In the states of Attached.SRC 0b: NOT in the states of Attached.SRC	0b
[2]	ACTIVECABLE	R	1b: R_a is detected when configured as Source 0b: Not Ra detected	0b
[1]	AUDIOVBUS	R	1b: In AudioAccessory State, VBUSOK=1 0b: NOT in AudioAccessory State	0b
[0]	AUDIO	R	1b: In AudioAccessory State, VBUSOK=0 0b: NOT in AudioAccessory State	0b

The INTERRUPT and INTERRUPT1 registers indicate one or some of the interruption are trigerred. Once the interruption bit is set, it is latched until the I^2C master writes 1b to this bit to clear it. If any interruptions list below is trigerred, the corresponding bit is set but this bit can be set by MASK and MASK1 registers to determine whether this interruption can assert the INT_N low to request the I^2C master's attention.

Table 28. INTERRUPT (Address: 0x14)

Bit		Field	Type	Description	Default
[7]		Reserved	R/W	Reserved	0b
[6]		I_ORIENT	R/W	1b: ORIENT in STATUS has changed from 00b to 01b, or 00b to 10b 0b: No such interruption occurs	0b
[5]		Reserved	R/W	Reserved	0b
[4]		I_VBUS_CHG	R/W R	1b: VBUSOK transitions from 0b to 1b or 1b to 0b 0b: No such interruption occurs	0b
[3]		I_AUTOSNK	R/W	1b: AUTOSNK function is enabled and it is activated or deactivated 0b: No such interruption occurs	0b
[2]		I_BC_LVL	R/W	1b: BC_LVL in STATUS is changed 0b: No such interruption occurs	0b
[1]		I_DETACH	R/W	1b: One of exit of Attached.SRC/Attached.SNK/ DebugAccessory.SNK/ AudioAccessory/UnorientedDebugAccessory.SRC/ OrientedDebugAccessory.SRC states happens 0b: No such interruption occurs	0b
[0]		I_ATTACH	R/W	1b: One of entry of Attached.SRC/Attached.SNK/ DebugAccessory.SNK/ AudioAccessory/UnorientedDebugAccessory.SRC/ OrientedDebugAccessory.SRC states happens 0b: No such interruption occurs	0b

Table 29. INTERRUPT1 (Address: 0x15)

Bit	Field	Type	Description	Default
[7:3]	Reserved	R/W	Reserved	00000b
[2]	I_FRC_FAIL	R/W	1b: FORCE_SRC or FORCE_SNK has failed 0b: No such interruption occurs	0b

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Bit	Field	Type	Description	Default
[1]	I_FRC_SUCC	R/W	1b: FORCE_SRC or FORCE_SNK has been done 0b: No such interruption occurs	0b
[0]	Reserved	R/W	Reserved	0b

The USER CFG register is an additional register where controls some functions in the HUSB320. Its default values is downloaded from FACTORY CONFIGURATION registers and may be changed by I²C master during normal operation.

Table 30. HUSB320-BAXXX USER CFG (Address: 0x16)

Bit	Field	Type	Description	Default
[7:6]	Reserved	R/W	Reserved	10b
[5]	CC_DSCNTEN	R/W	In Attached.SNK, connected CC is used to monitor the disconnection 0b:Disabled 1b:Enabled	0b
[4]	Reserved	R/W	Reserved	1b
[3:2]	TVBDSGTIMEOUT	R/W	Max conduction time of VBUS_DSG=1b 00b: Disable VBUS_DSG always 01b:15 ms 10b: 50 ms 11b:100 ms	00b
[1:0]	TBC_LEVEL	R/W	Debounce time of BC_LVL change 00b: 0.5 ms 01b: 3 ms 10b: 12 ms 11b: 18 ms	10b

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TYPICAL APPLICATION CIRCUITS

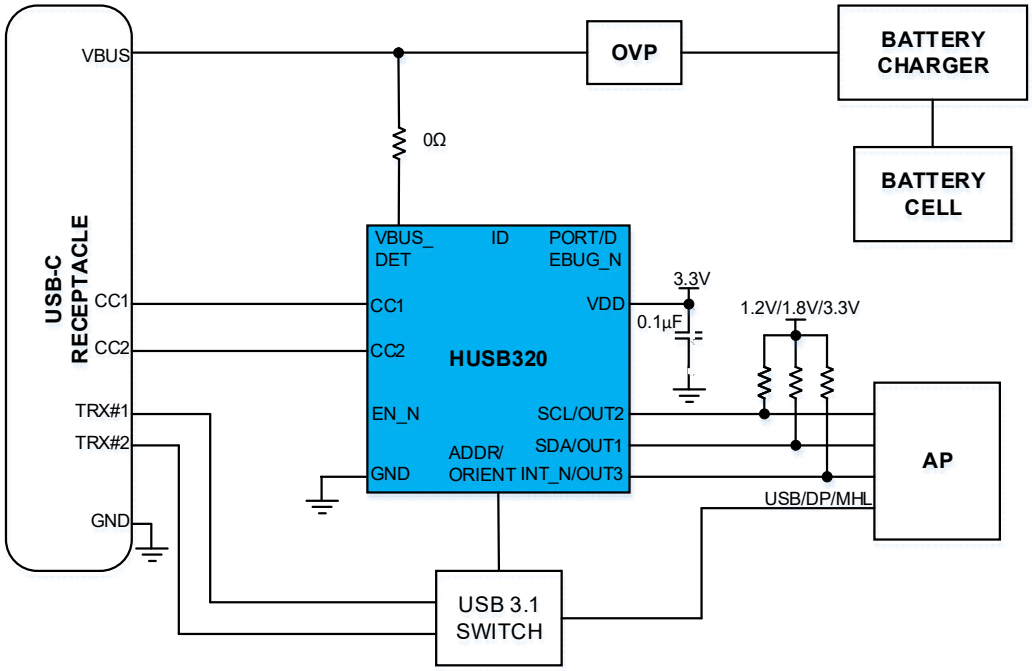


Figure 10. HUSB320-BA000-QN12R Typical Application

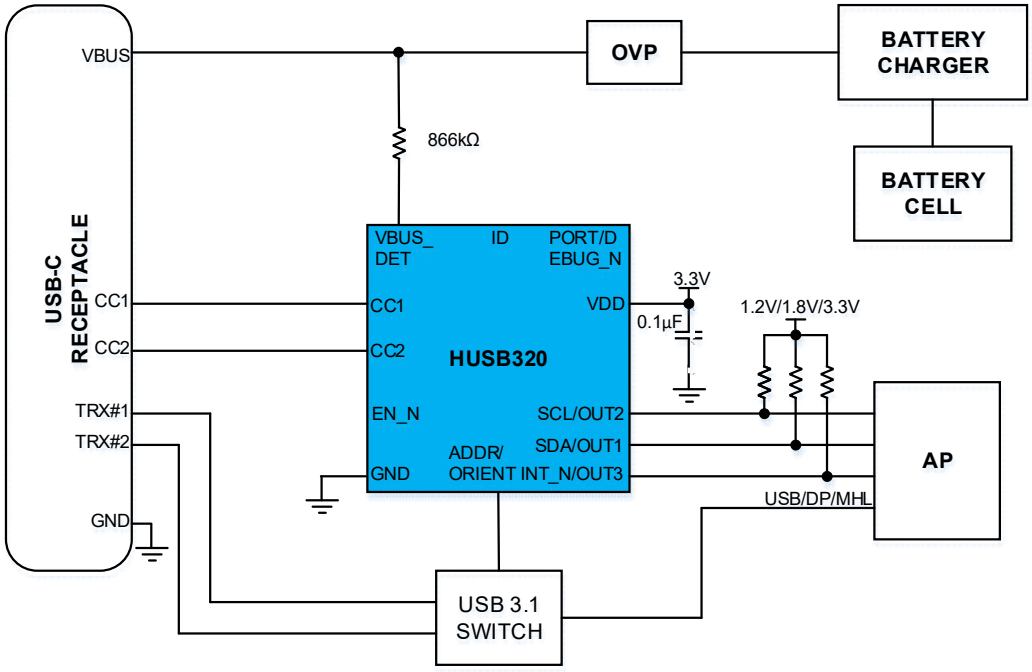
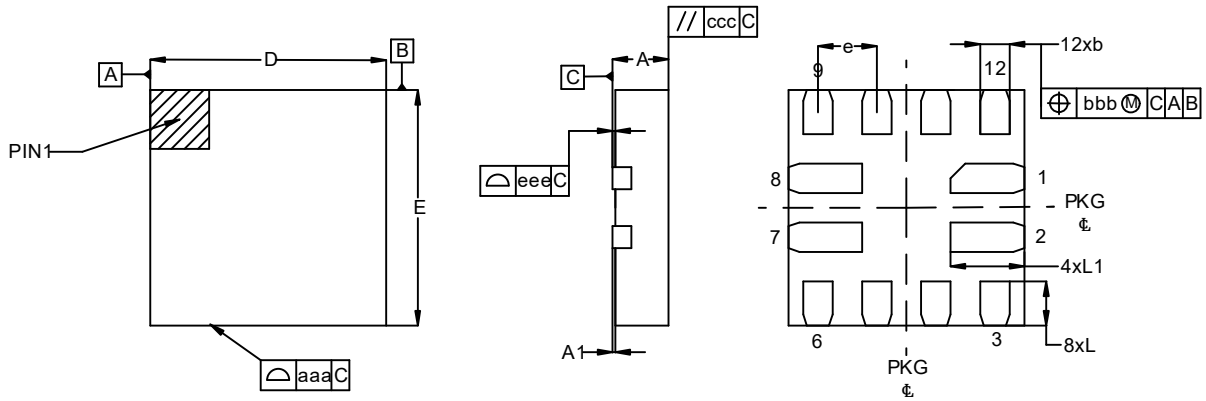


Figure 11. HUSB320-BA001-QN12R Typical Application

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PACKAGE OUTLINE DIMENSIONS



TOP VIEW SIDE VIEW BOTTOM VIEW

	DIMENSION IN MILLIMETERS		
SYMBOLS	MIN	NOM	MAX
A	0.31	0.37	0.40
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		1.60 BSC	
E		1.60 BSC	
e		0.40 BSC	
L	0.25	0.30	0.35
L1	0.45	0.50	0.55
aaa		0.10	
bbb		0.07	
ccc		0.10	
eee		0.08	

Figure 12. QFN1.6x1.6-12L Package of Dimension

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PACKAGE TOP MARKING

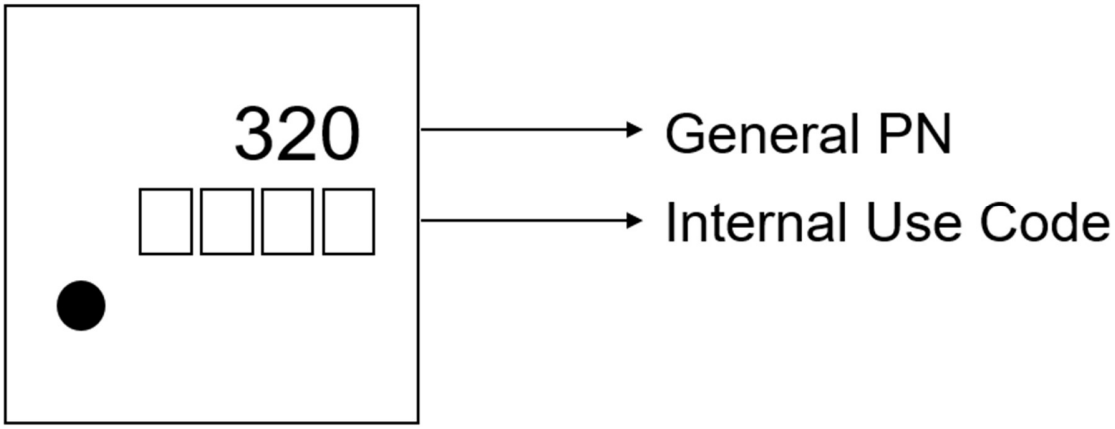


Figure 13. Package Top Marking

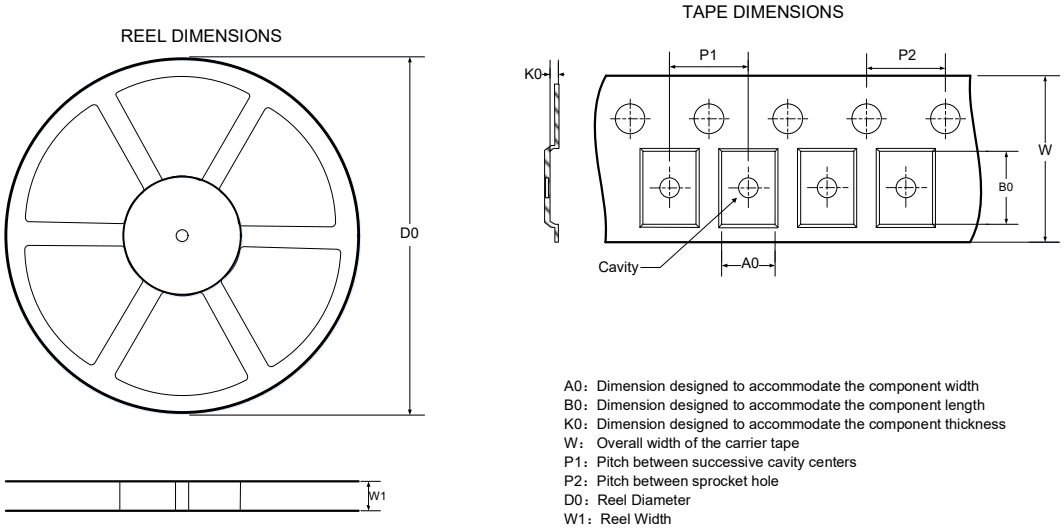
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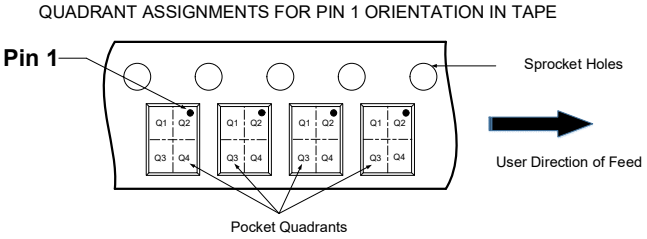
ORDERING GUIDE

Model	Configurations	T_J Temp (°C)	Package Type	Package Option
HUSB320-BA000-QN12R	VBUS_DET pin External resistor 0 Ω ; Disable the ADDR and PORT pin output modes	-40 to 125	QFN1.6x1.6-12L	T&R, 3k
HUSB320-BA001-QN12R	VBUS_DET pin External resistor 866 kΩ ; Disable the ADDR and PORT pin output modes	-40 to 125	QFN1.6x1.6-12L	T&R, 3k

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TAPE AND REEL INFORMATION





DIMENSIONS AND PIN1 ORIENTATION

D0 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant	Quantity
178.00	9.50	1.80	1.80	0.45	4.00	4.00	8.00	Q2	3000

All dimensions are nominal

Figure 14. Tape and Reel Information

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